DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE MATERIALS

CS 207 ELECTRONIC DEVICES & CIRCUITS

VISION OF THE INSTITUTION

To mould true citizens who are millennium leaders and catalysts of change through excellence in education.

MISSION OF THE INSTITUTION

NCERC is committed to transform itself into a center of excellence in Learning and Research in Engineering and Frontier Technology and to impart quality education to mould technically competent citizens with moral integrity, social commitment and ethical values.

We intend to facilitate our students to assimilate the latest technological know-how and to imbibe discipline, culture and spiritually, and to mould them in to technological giants, dedicated research scientists and intellectual leaders of the country who can spread the beams of light and happiness among the poor and the underprivileged.

ABOUT DEPARTMENT

- Established in: 2002
- Course offered : B.Tech in Computer Science and Engineering

  M.Tech in Computer Science and Engineering

  M.Tech in Cyber Security
- Approved by AICTE New Delhi and Accredited by NAAC
- Affiliated to the University of A P J Abdul Kalam Technological University.

DEPARTMENT VISION

Producing Highly Competent, Innovative and Ethical Computer Science and Engineering Professionals to facilitate continuous technological advancement.

DEPARTMENT MISSION

1. To Impart Quality Education by creative Teaching Learning Process
2. To Promote cutting-edge Research and Development Process to solve real world problems with emerging technologies.
3. To Inculcate Entrepreneurship Skills among Students.
4. To cultivate Moral and Ethical Values in their Profession.
5.

PROGRAMME EDUCATIONAL OBJECTIVES

PEO1: Graduates will be able to Work and Contribute in the domains of Computer Science and Engineering through lifelong learning.

PEO2: Graduates will be able to Analyse, design and development of novel Software Packages, Web Services, System Tools and Components as per needs and specifications.

PEO3: Graduates will be able to demonstrate their ability to adapt to a rapidly changing environment by learning and applying new technologies.

PEO4: Graduates will be able to adopt ethical attitudes, exhibit effective communication skills, Teamworkand leadership qualities.

PROGRAM OUTCOMES (POS)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO1: Ability to Formulate and Simulate Innovative Ideas to provide software solutions for Real-time Problems and to investigate for its future scope.

PSO2: Ability to learn and apply various methodologies for facilitating development of high quality System Software Tools and Efficient Web Design Models with a focus on performance

optimization.

PSO3: Ability to inculcate the Knowledge for developing Codes and integrating hardware/software products in the domains of Big Data Analytics, Web Applications and Mobile Apps to create innovative career path and for the socially relevant issues.

COURSE OUTCOMES

CO1	To introduce to the students the fundamental concepts of electronic devices and circuits for engineering applications.
CO2	To develop the skill of analysis and design of various analog circuits using electronic devices
CO3	To provide comprehensive idea about working principle, operation and applications of electronic circuits
CO4	To equip the students with a sound understanding of fundamental concepts of operational amplifiers
CO5	To expose to the diversity of operations that operational amplifiers can perform in a wide range of applications
CO6	To expose to a variety of electronic circuits/systems using various analog ICs

MAPPING OF COURSE OUTCOMES WITH PROGRAM OUTCOMES

	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**
CO1	3		3	2	2	2			2			
CO2	3	3	3	2	2	2			2			
CO3	3	3	3	2	2	2			2			
CO4	3	3	3	2	2	2			2			
CO5	3	3	3	2	2	2			2			
CO6	3	3	3	2	2	2			2			

Note: H-Highly correlated=3, M-Medium correlated=2, L-Less correlated=1

PSO MAPPINGS ALSO NEEDS TO INCLUDE

CO'S	PSO1	PSO2	PSO3
C205.1	3	3	2
C205.2	3	3	2
C205.3	3	3	2
C205.4	3	3	2
C205.5	3	3	2
C205.6	3	3	2

SYLLABUS

Course code	Course Name	L-T-P -Credits	Year of Introduction
CS207	ELECTRONIC DEVICES & CIRCUITS	3-0-0-3	2016

Pre-requisite: BE101-04 Introduction to Electronics Engg.

Course Objectives:

1. To introduce to the students the fundamental concepts of electronic devices and circuits for engineering applications
2. To develop the skill of analysis and design of various analog circuits using electronic devices
3. To provide comprehensive idea about working principle, operation and applications of electronic circuits
4. To equip the students with a sound understanding of fundamental concepts of operational amplifiers
5. To expose to the diversity of operations that operational amplifiers can perform in a wide range of applications
6. To expose to a variety of electronic circuits/systems using various analog ICs

Syllabus

RC Circuits, Diode Circuits, Regulated power supplies, **Field effect transistor**, DC analysis of BJT, RC Coupled amplifier, MOSFET amplifiers, Feedback amplifiers, Power amplifiers, Oscillators, Multivibrators, Operational Amplifier and its applications, Timer IC.

Expected Outcome:

Students will be able to

1. explain, illustrate, and design the different electronic circuits using electronic components
2. design circuits using operational amplifiers for various applications

Text Books:

1. David A Bell, Electronic Devices and Circuits, Oxford University Press, 2008
2. Salivahanan S. and V. S. K. Bhaaskaran, Linear Integrated Circuits, Tata McGraw Hill, 2008

References :

1. Neamen D., Electronic Circuits, Analysis and Design, 3/e, TMH, 2007
2. Robert Boylestad and L Nashelsky, Electronic Devices and Circuit Theory, Pearson.
3. Bogart T. F., Electronic Devices Circuits, 6/e, Pearson, 2012.
4. Maini A. K. and V. Agrawal, Electronic Devices and Circuits, Wiley India, 2011.
5. K.Gopakumar, Design and Analysis of Electronic Circuits, Phasor Books, Kollam, 2013
6. Millman J. and C. Halkias, Integrated Electronics, 2/e, McGraw-Hill, 2010.

Course Plan

Module	Contents	Hours (40)	Sem Exam Marks
1	**Wave shaping circuits:** Sinusoidal and non-sinusoidal wave shapes, Principle and working of RC differentiating and integrating circuits, Conversion of one non-sinusoidal wave shape into another. Clipping circuits - Positive, negative and biased clipper.	5	15%
	Clamping circuits - Positive, negative and biased clamper. Voltage multipliers- Voltage doubler and tripler. Simple sweep circuit using transistor as a switch.		
2	**Regulated power supplies:** Review of simple zener voltage regulator, Shunt and series voltage regulator using transistors, Current limiting and fold back protection, 3 pin regulators-78XX and 79XX, IC 723 and its use as low and high voltage regulators, DC to DC conversion, Circuit/block diagram and working of SMPS.	4	15 %
	Field effect transistors: JFET – Structure, principle of operation and characteristics, Comparison with BJT. MOSFET- Structure, Enhancement and Depletion types, principle of operation and characteristics.	3	
	FIRST INTERNAL EXAM		
3	**Amplifiers:** Introduction to transistor biasing, operating point, concept of load line, thermal stability, fixed bias, self bias, voltage divider bias. Classification of amplifiers, RC coupled amplifier - voltage gain and frequency response. Multistage amplifiers - effect of cascading on gain and bandwidth. Feedback in amplifiers - Effect of negative feedback on amplifiers. MOSFET Amplifier- Circuit diagram and working of common source MOSFET amplifier.	7	15 %

4	**Oscillators:** Classification, criterion for oscillation, analysis of Wien bridge oscillator, Hartley and Crystal oscillator. Non-sinusoidal oscillators: Astable, monostable and bi-stable multivibrators using transistors (Only design equations and working of circuit are required, Analysis not required).	5	15 %
	SECOND INTERNAL EXAM		
5	**Operational amplifiers:** Differential amplifier, characteristics of op-amps(gain, bandwidth, slew rate, CMRR, offset voltage, offset current), comparison of ideal and practical op-amp(IC741), applications of op-amps- scale changer, sign changer, adder/summing amplifier, subtractor, integrator, differentiator, Schmitt trigger, Wien bridge oscillator.	8	20 %
6	**Integrated circuits:** Active filters – Low pass and high pass (first and second order) active filters using op-amp with gain (No analysis required). D/A and A/D convertors – important specifications, Sample and hold circuit. Binary weighted resistor and R-2R ladder type D/A convertors. (concepts only). Flash, dual slope and successive approximation type A/D convertors. Circuit diagram and working of Timer IC555, astable and monostablemultivibrators using 555.	8	20 %
	END SEMESTER EXAM		

Question Paper Pattern:

1. There will be *five* parts in the question paper – A, B, C, D, E
2. Part A
   a. Total marks : 12
   b. *Four* questions each having 3 marks, uniformly covering module I and II; All *four* questions have to be answered.
3. Part B
   a. Total marks : 18
   b. *Three* questions each having 9 marks, uniformly covering module I and II; Two questions have to be answered. Each question can have a maximum of three subparts
4. Part C
   a. Total marks : 12
   b. *Four* questions each having 3 marks, uniformly covering module III and IV; All *four* questions have to be answered.
5. Part D
   a. Total marks : 18
   b. *Three* questions each having 9 marks, uniformly covering module III and IV; Two questions have to be answered. Each question can have a maximum of three subparts
6. Part E
   a. Total Marks: 40
   b. *Six* questions each carrying 10 marks, uniformly covering modules V and VI; *four* questions have to be answered.
   c. A question can have a maximum of three sub-parts.
7. There should be at least 60% analytical/numerical/design questions.

QUESTION BANK

MODULE I				
Q:NO:	**QUESTIONS**	**CO**	**KL**	**PAGE NO:**
1	Describe about **non-linear wave shaping.**	CO1	K2	1
2	**Discuss about non-linear network.**	CO1	K3	3
3	**List out the applications of voltage comparator.**	CO1	K3	4
4	**Explain the operation of positive clamper (Negative peak clamper).**	CO1	K2	7
5	**Explain the operation of negative clamper (positive peak clamper).**	CO1	K2	8
6	**Explain the working of RC low pass filter, how it can be act as an integrator.**	CO1	K2	3
7	**Explain the working of RC high pass filter, how it can be act as an differentiator.**	CO1	K2	4
8	**Explain about Sweep circuits? Explain the working of a simple sweep circuit using transistor as a switch with relevant sketches.**	CO1	K2	12
9	**Explain the working of Voltage Doubler/Tripler/Quadruppler with help of a neat sketch.**	CO1	K2	10
10	**Explain the working of Clamper Circuits with Diagrams.**	CO1	K2	8
11	**Explain the working of Clipping Circuits with Diagrams.**	CO1	K2	7

	MODULE II			
1	**Expain unregulated power supply is not good ?enough for many applications in electronics?**	CO2	K2	13
2	**Discuss about series voltage regulators are called Linear voltage regulators?**	CO2	K2	22
3	**List out the limitations of series Voltage regulators**?	CO2	K3	20
4	**Explain why BJT is called bipolar device while FETs are called Unipolar device?**	CO2	K4	21
5	**Draw the circuit diagram of Zener-voltage regulator and explain how line & Load regulation is achieved in the circuit.**	CO2	K3	12
6	**Explain with diagram the fold back current limiting circuit.**	CO2	K2	25
7	**Explain how short circuit & overload protection is achieved in series voltage regulators.**	CO2	K2	26
8	**Explain with sketches the working of IC 723 as Low & high Voltage regulator.**	CO2	K2	32
9	**Draw the block diagram & Explain 3 terminal voltage regulators.**	CO2	K4	33
10	**Explain with diagram the functioning of SMPS.**	CO2	K2	35
11	**Define pinch –off voltage of a JFET and explain its significance?**	CO2	K1	32
12	**Draw the Structural diagram of MOSFET and explain its operation.**	CO2	K2	36
13	**Draw the Structural diagram of N- Channel JFET and explain its operation.**	CO2	K2	37
	MODULE III			
1	**Define Stability factor & derive the general expression for stability factor.**	CO3	K1	53
2	**Discuss about multistage amplifier circuit?**	CO3	K3	62
3	**Explain about cascaded amplifiers? Explain the**	CO3	K2	63

	effect of cascading on Gain & Bandwidth.			
4	**Draw fixed Biased circuit & derive its Stability factor.**	CO3	K3	54
5	Expain about voltage divider bias circuit.Derive the expression for stability factor	CO3	K4	55
6	Expain about dc load and ac load line	CO3	K2	56
7	Expalin detail about multistage amplifiers	CO3	K2	67
8	Draw the neat diagram of common source amplifier with neat diagram	CO3	K3	67
9	Expain about effect of negative feed back on amplifier	CO3	K2	68
10	Draw the circuit dagram of direct coupled amplifier,Explain its working	CO3	K3	69
	MODULE IV			
1	**Draw the circuit & explain the working of Wein bridge oscillator. Also derive its frequency of operation.**	CO4	K3	78
2	**Explain the concept involved in crystal oscillator with its characteristics?**	CO4	K2	78
3	**Explain Bistable Multivibrator**	CO4	K2	85
4	**Explain about collector coupled Astable Multivibrator**	CO4	K2	86
5	**Explain emitter coupled Astable Multivibrator**	CO4	K2	87
6	**Draw and explain a one-shot circuit.**	CO4	K2	86
7	**Discuss the conditions for sustained oscillator or what is Barkhausen criterion?**	CO4	K3	77
8	**List out the classifications of Oscillators?**	CO4	K3	76

9	**Explain types of feedback oscillators?**	CO4	K2	77
10	**List the conditions for oscillation?**	CO4	K2	78
11	**Define Piezoelectric effect.**	CO4	K1	85
12	**Explain Miller crystal oscillator? Explain its operation.**	CO4	K2	86
	MODULE V			
1	**Compare ideal and practical Op-Amp parameters**	CO5	K3	94
2	**Explain Slew Rate & what causes slew rate.**	CO5	K2	95
3	**Explain the application Op-Amp as Sign Changer & Scale Changer.**	CO5	K3	96
4	**Write Notes on Integrator & Differentiator using Op-Amp.**	CO5	K3	97
5	**Explain the application Op-Amp as Summing & Difference Amplifier**	CO5	K2	98
6	**Draw and explain Schmitt trigger Using Opamp**	CO5	K3	104
7	**Draw the circuit diagram of Wien bridge oscillator Using Op amp & Explain its operation.**	CO5	K3	108
	MODULE VI			
1	**List-out the Advantages & Disadvantages of Active filters over Passive filters.**	CO6	K3	110
2	**Explain about Butterworth filters? Explain its Ist order LP & HP filters.**	CO6	K2	111
3	**Draw and explain 2nd order Butterworth LPF & HPF**	CO6	K2	114
4	**Explain with a diagram the principle of working of Sample & Hold Circuit.**	CO6	K2	115
5	**List out the specifications of Digital to Analog Converters**	CO6	K3	118

6	**Explain the working of Dual slope ADC with the help of a Diagram**	CO6	K2	120
7	**Explain the working of SAR & Flash type ADCs with the help of a Diagram**	CO6	K2	121
9	**Draw the Functional block Diagram of 555 Timer IC and Explain its operation as Astable-Multi vibrator.**	CO6	K3	129
10	**Draw the Diagram of Monostable Multi-vibrator using 555 IC and explain its operation**	CO6	K3	130
11	**Design a Butterworth LPF having Cutoff frequency of 2 KHz and pass band gain of 2.5**	CO6	K5	132
12	**Design a second order LPF at cutoff frequency 1KHz**	CO6	K5	134
13	**Determine the resolution of a). 6 Bit DAC b). 12 Bit DAC in terms of percentage**	CO6	K5	134
14	**Design a 4 bit weighted Resistor DAC whose full scale output voltage is -5V.logic levels are 1= +5V; 0= -5V.What is the output voltage when input voltage is 1101**	CO6	K5	135
15	**An 8 bit DAC produce Vout = 0.05V for a Digital input of 00000001.Find full scale output. What is its resolution. What is output for an input of 00101010**	CO6	K5	135

APPENDIX 1

CONTENT BEYOND THE SYLLABUS

S:NO;	TOPIC	PAGE NO:
1	PCB DESIGN	139

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MODULE 1

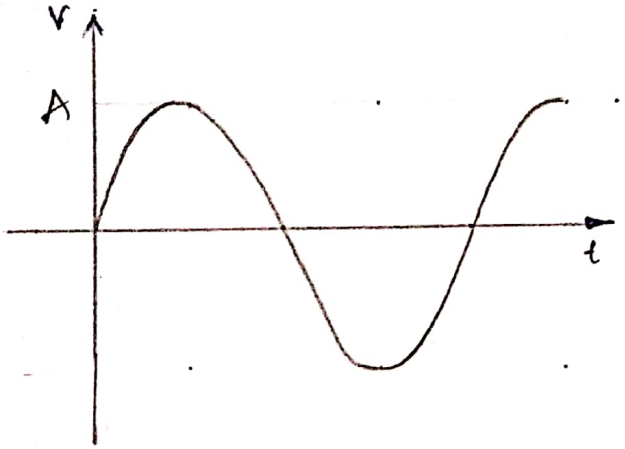
MODULE II

(1)

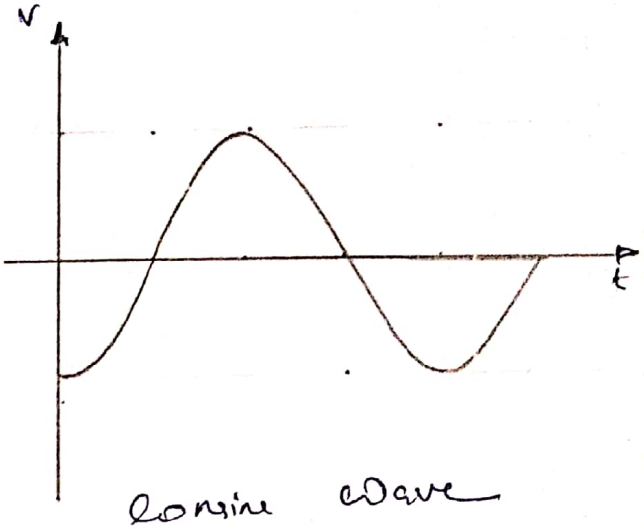
: WAVE SHAPING CIRCUITS:

Sinusoidal & Non-Sinusoidal Wave Shapes:

A Sine wave or Sinusoid is a mathematical curve that describes a smooth repetitive oscillation. usually with time as the independent variable. A cosine wave is a sinusoidal. it has the same form but it has been phase shifted by 90°.



Sine wave

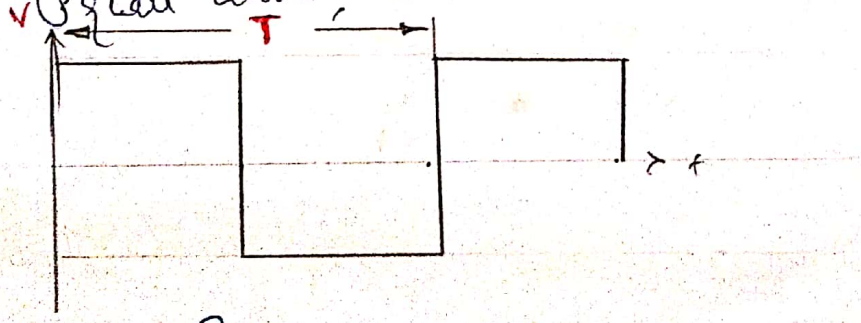


Cosine wave

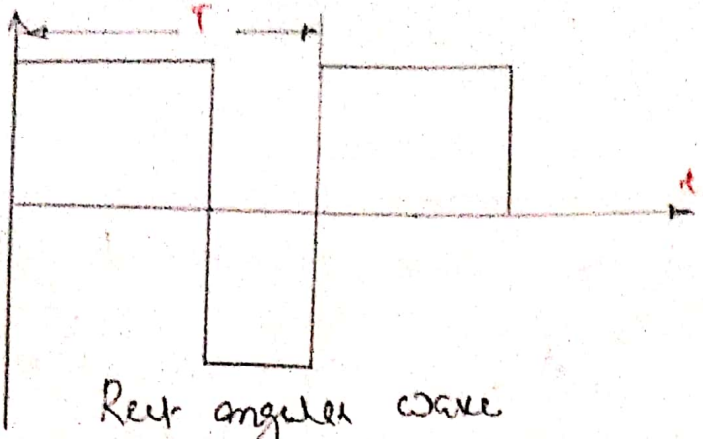
$y(t) = A \sin \omega t$

A = Amplitude
ω = Angular frequency.

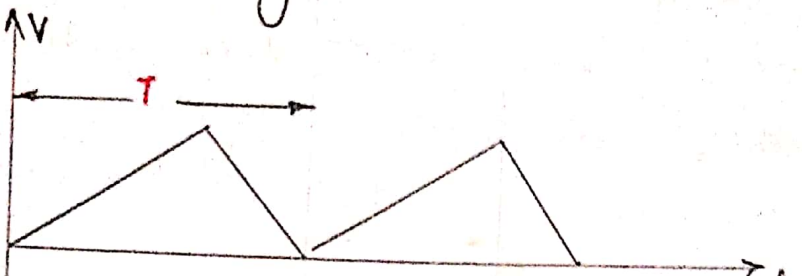
A non sinusoidal waveform is one that is not a sine wave. and its examples are triangular, rectangular, square wave, pulse etc



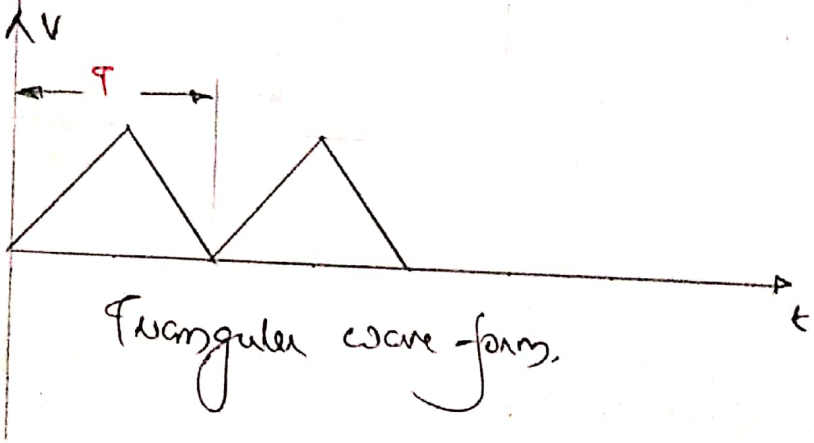
Square wave



Rectangular wave



Saw tooth wave



Triangular wave-form.

$x_c = \frac{1}{2\pi f c}$

$T \geq 10 \, RC$

Differentiating & Integrating Circuit:

Differentiating Circuit:

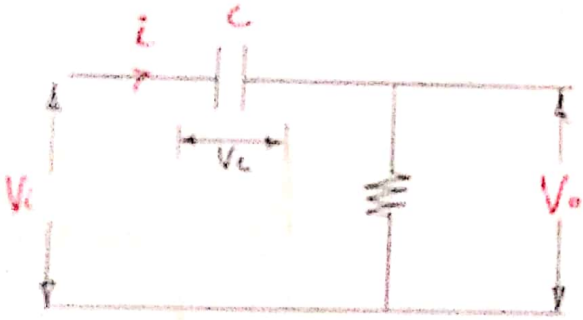
(2)

A circuit in which o/p voltage is directly proportional to the derivative of input is known as differentiating circuit.

$$\text{Output} \propto \frac{d}{dt}(\text{input})$$

A differentiating ckt is a simple RC circuit where the o/p is taken across the resistor R.

If a dc or constant input is applied to such a ckt, the o/p will be zero.



In order to achieve good differentiation, the following two conditions should be satisfied.

1. The time constant RC of ckt should be much smaller than the time period of input wave.
2. The value of X_C should be 10 or more times smaller than R at operating frequency. $X_C \geq 10R$.

If these conditions are fulfilled then the o/p across R will be derivative of the input.

Let Vi be input voltage & i be i/p current

Now charge of capacitor is

$$Q = CV_c$$

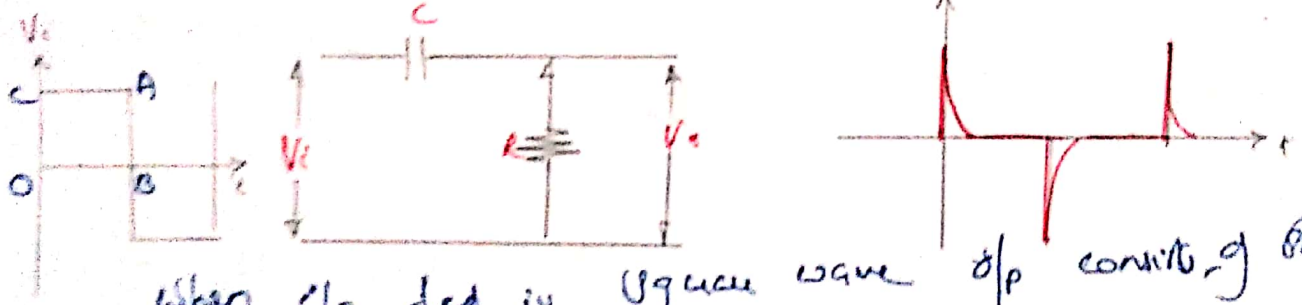
Now $$i = \frac{dq}{dt} = \frac{d}{dt}(Q) = \frac{d}{dt} CV_c$$

Since capacitive reactance is much larger than R i/p voltage can be considered equal to capacitor voltage $V_c = V_i$

So $$i = C \frac{dV_{in}}{dt}$$

$$\boxed{V_o = iR = RC \frac{dV_{in}}{dt}}$$ ∴ o/p ∝ $\frac{d}{dt}$ (input)

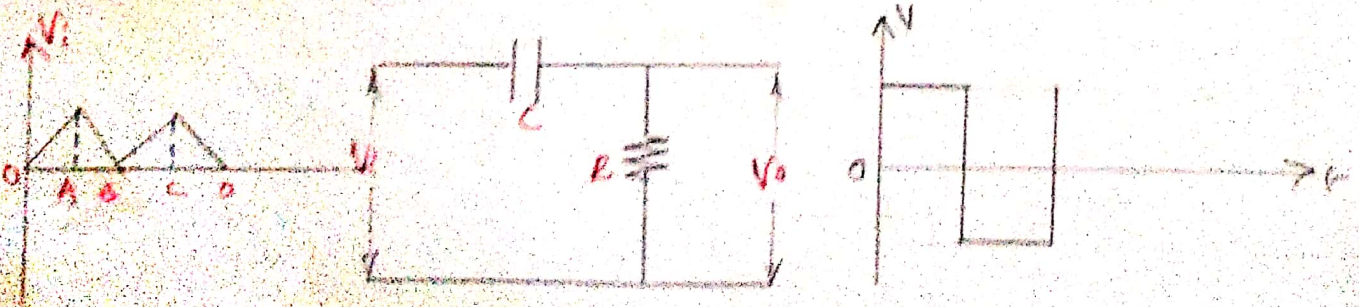
when i/p is Square wave



when i/p to is square wave o/p consists of sharp narrow pulses.

During dc part of input wave amplitude changes abruptly and hence differentiated o/p will be sharp pulses during const part CB of input o/p will be zero because derivative of const is zero.

when i/p is Triangular wave:



During AB period OA of input wave its amplitude changes at const. rate and uniform differentiated value is a const. for const rate of change.

During period BC of i/p wave, amplitude changes at a -ve constant rate and so differentiated wave has a -ve const value for negative const rate of change. (3)

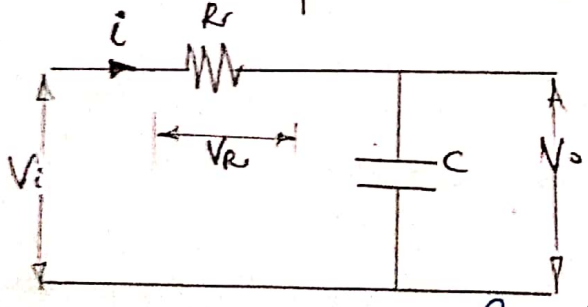
When i/p is Sine wave:

When i/p fed is Sine wave o/p will be a Cosine wave.

RC integrator Circuit:

A Circuit in which o/p voltage is directly proportional to integral of input is known as an integrating Circuit

$$\text{Output} \propto \int(\text{input})$$



In Order to achive good integrator

1. The time const. RC should be very large compared to time period of input wave
2. The value of R should be 10 or more times X_C

$$R \geq 10 X_C.$$

Let V_i = input voltage

Since $R \gg X_C$ $\quad V_R = V_i$

$i = \frac{V_R}{R} = \frac{V_i}{R}$

Charge q on capacitor

$$q = \int i\,dt$$

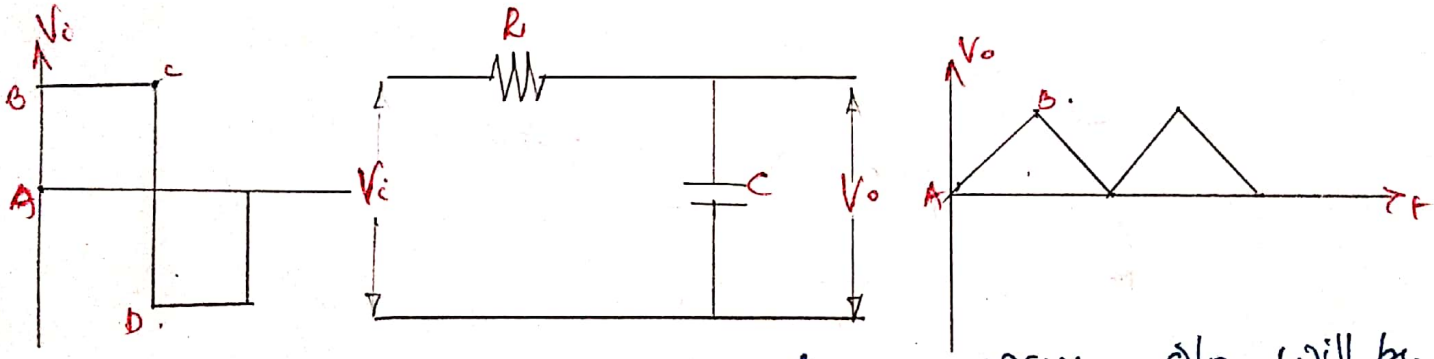
$\therefore$ o/p Voltage $V_o = \frac{q}{C} = \frac{\int i\,dt}{C}$

$$= \frac{\int \frac{V_i}{R}\,dt}{C}$$

$$\boxed{V_o = \frac{1}{RC}\int V_i\,dt}$$

i $V_o \propto \int V_i\,dt$

When i/p is Square wave:



when input fed is Square wave, o/p will be Triangular wave.

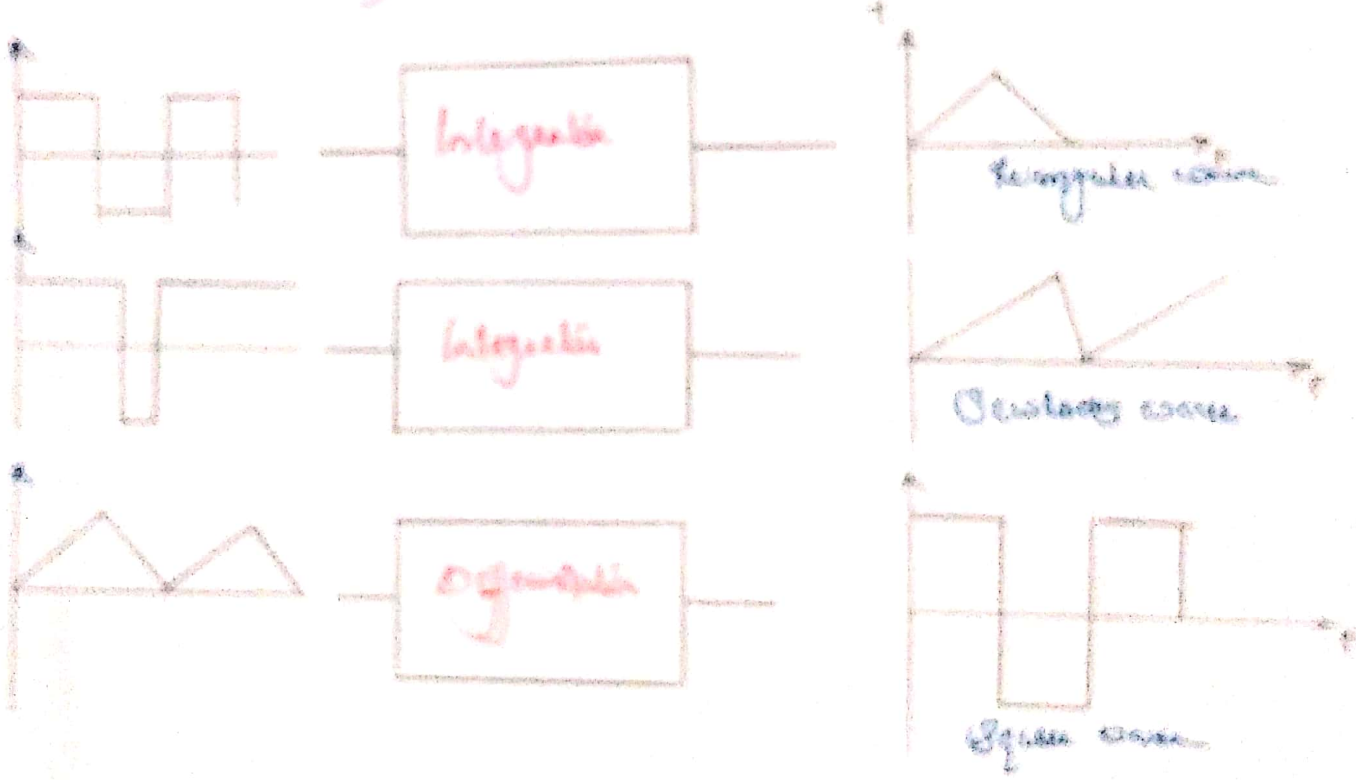
An integration means Summation; $\therefore$ o/p wave form will be Sum of input waves at any instant.

This Sum is Zero at A and goes on increasing till it becomes maximum at C. After this Summation goes on decreasing to the onset of -ve movement of input.

When I/p is Rectangular wave

When input fed is a rectangular wave o/p will be a triangular wave.

Conversion of Non-sinusoidal wave shape into another



: CLIPPING CIRCUITS: (5)

A wave shaping circuit which controls the shape of o/p wave form by removing or clipping a portion of applied wave is known as clipping circuit.

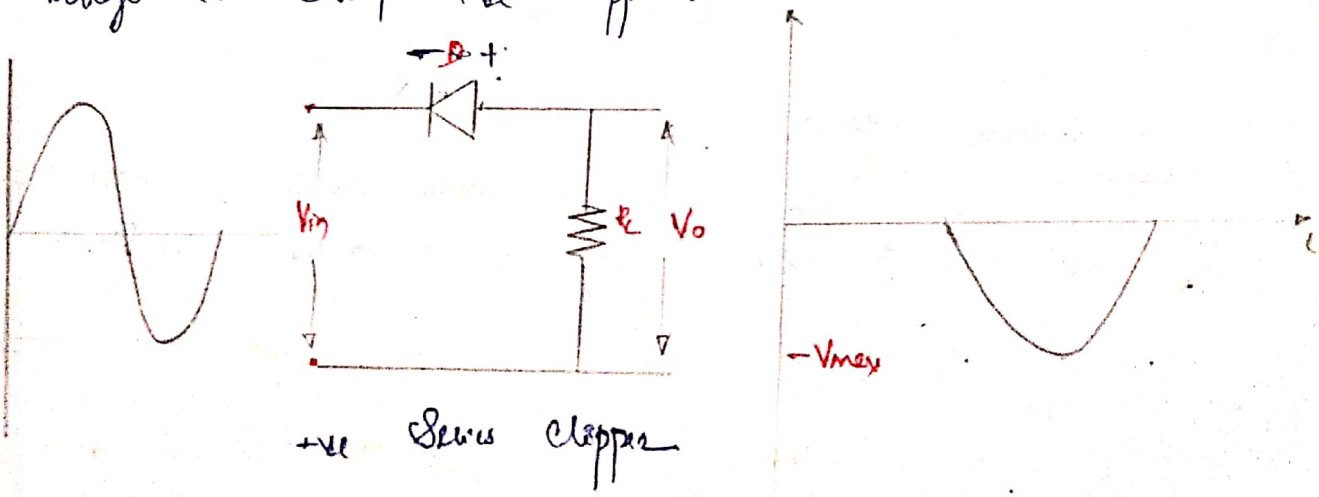
Hay wave rectifier is an example for clipper.

* According to configuration used:
  - Series diode clipper
  - Shunt or parallel diode clipper
  - combination of diode, resistance & power supply.

Key point: When a diode is connected in series with the load then ckt is called series clipper. & when the diode is connected on a branch which is parallel to the load it is called Parallel clipper.

Positive Clipper:

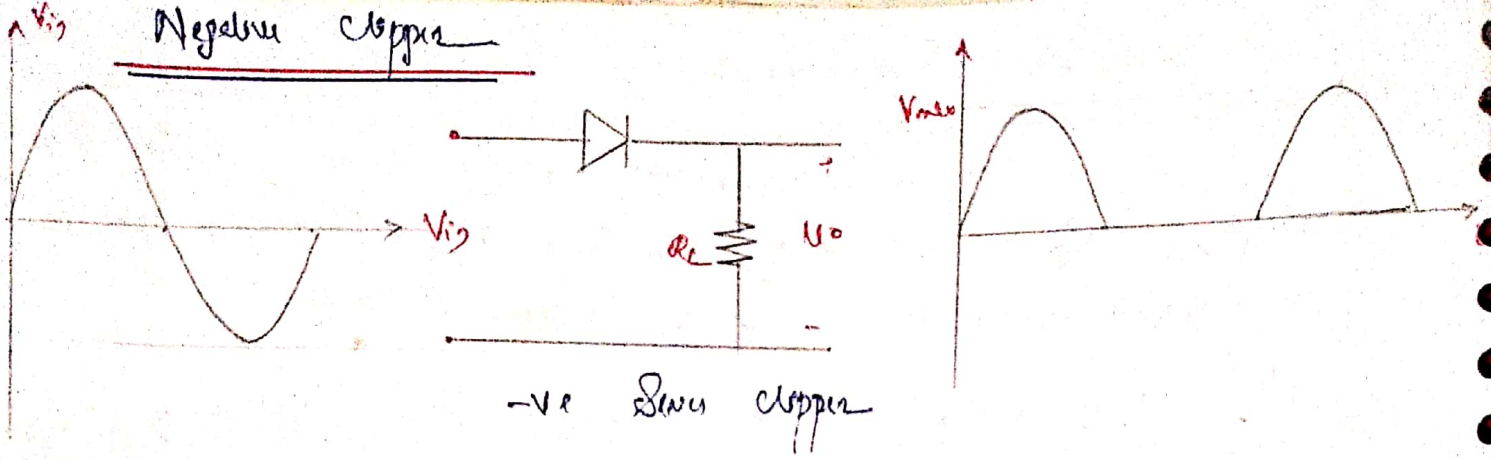
A clipper which removes the +ve hay cycle of input voltage is called +ve clipper:



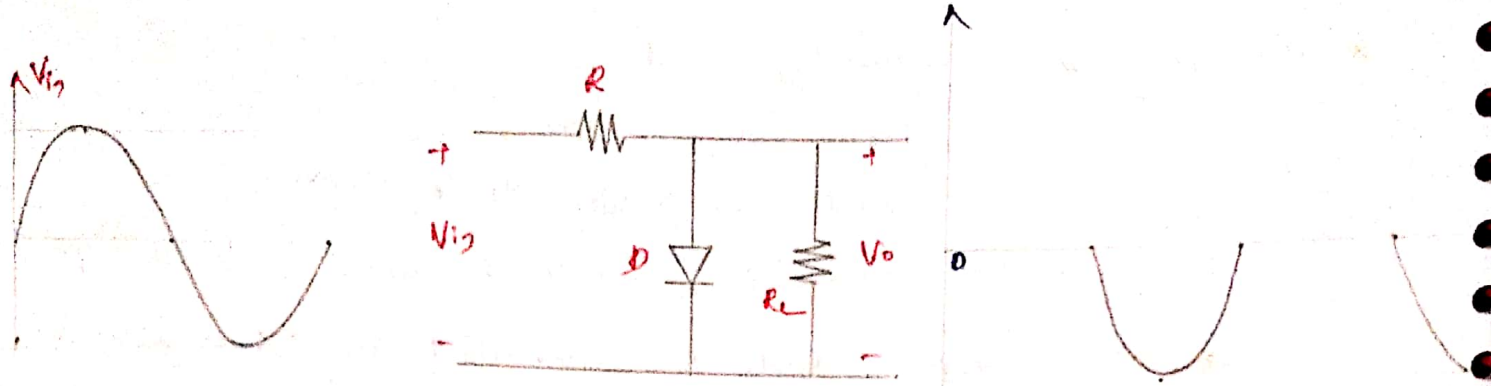
+ve Series clipper

When the i/p is positive diode D is reverse biased and o/p remains zero, & +ve hay cycle is clipped off During -ve hay cycle of input diode is forward biased and -ve hay cycle appears across o/p.

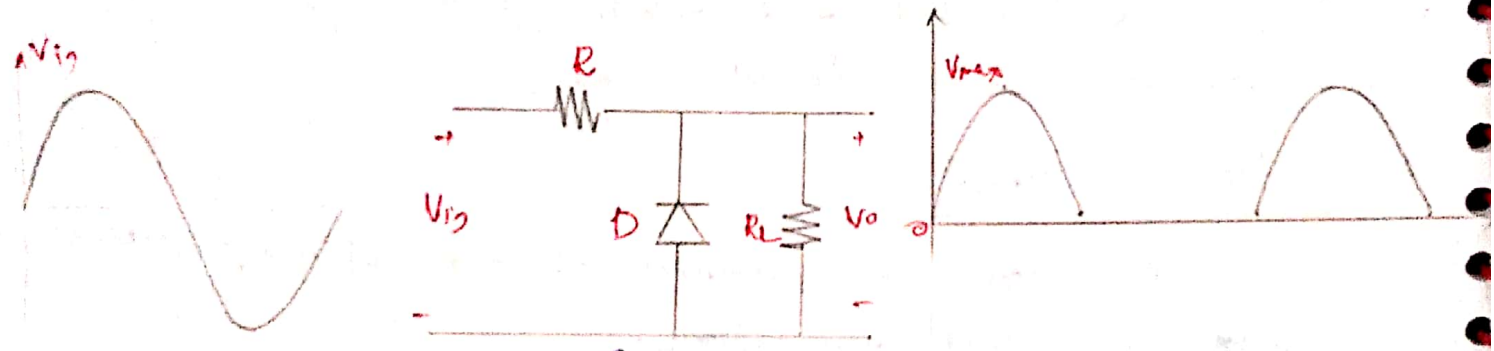
Negative clipper



-ve Series clipper



+ve Shunt clipper



-ve Shunt clipper

Biased clipper:

Inorder to remove a small portion of +ve or -ve half cycle of input voltage biased clippers are used

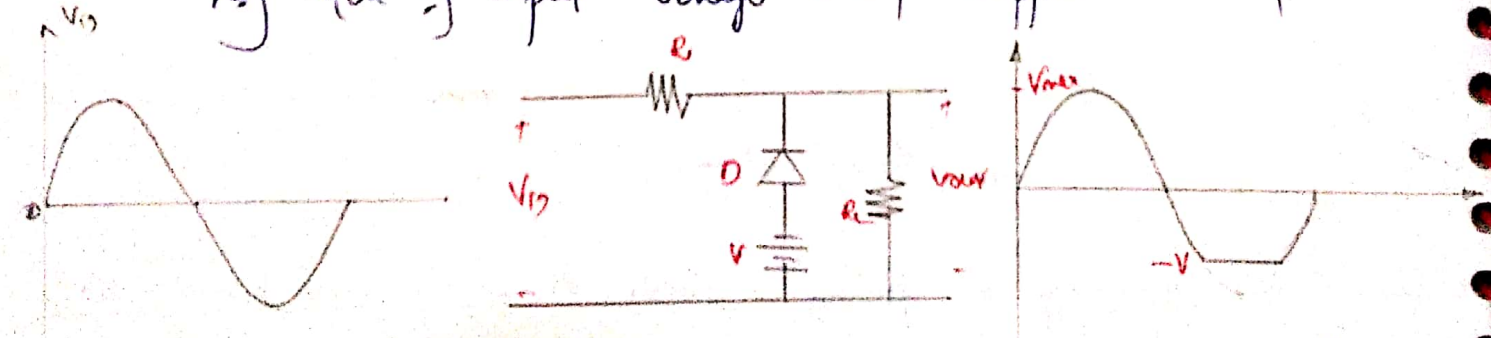
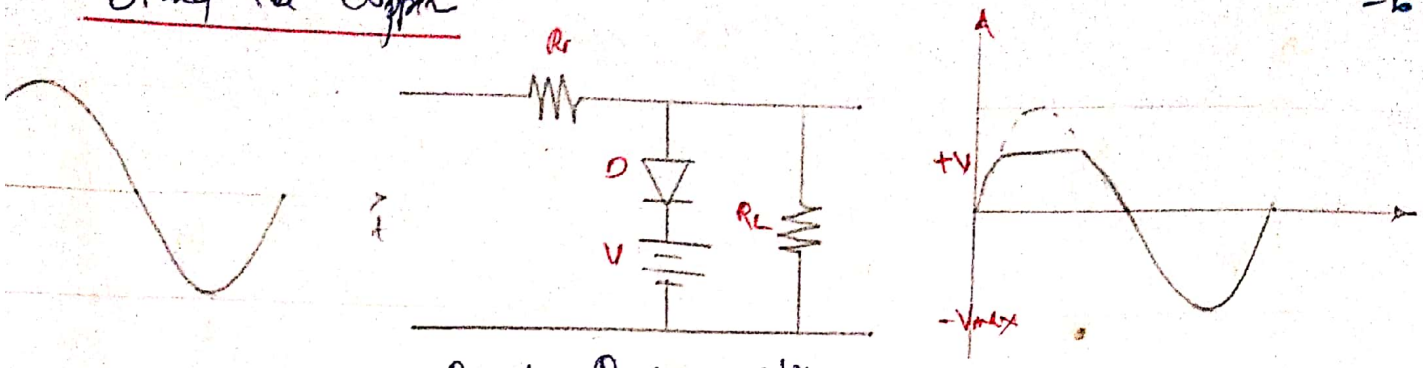


Figure shows negative clipping circuit which clips the -ve going half cycle at a -ve voltage when the voltage is above -V, diode D is reverse biased and hence the o/p voltage is same as the input voltage otherwise, the diode is forward biased and waveform gets clipped

Biased type clipper

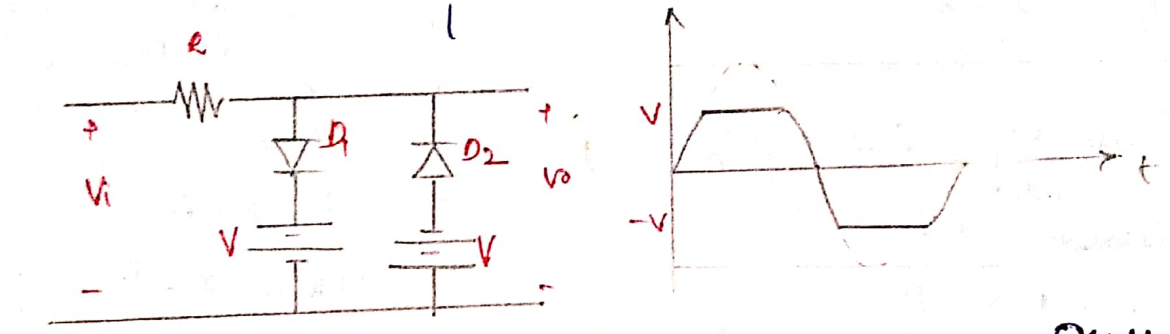


Biased Positive clipper.

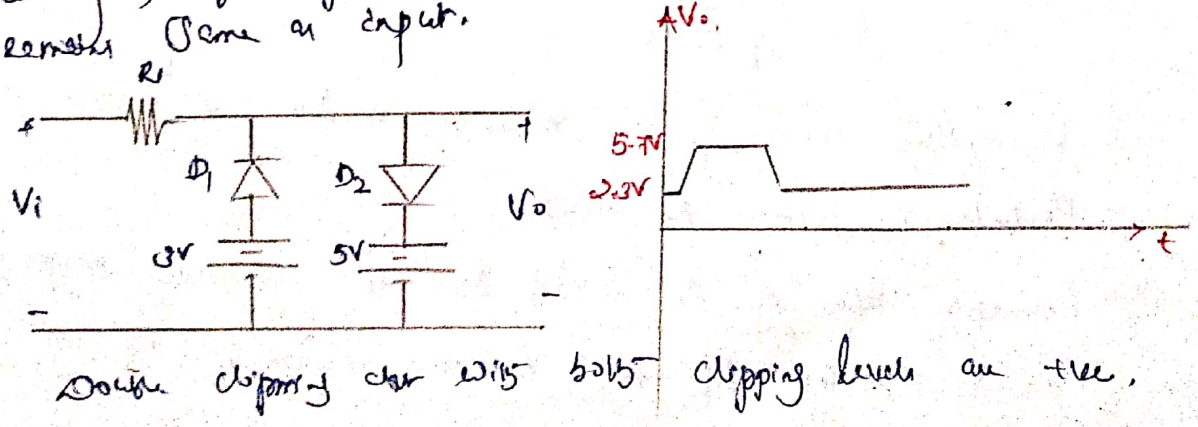
Up to the point when i/p voltage is equal to voltage V the diode is reverse biased and o/p is same as i/p. And when input voltage is above +V in positive half cycle diode is forward biased and become short ckt. Also the o/p is equal to +V. In -ve half cycle diode is reverse biased and o/p is equal to input.

(6)

Double clipping circuit

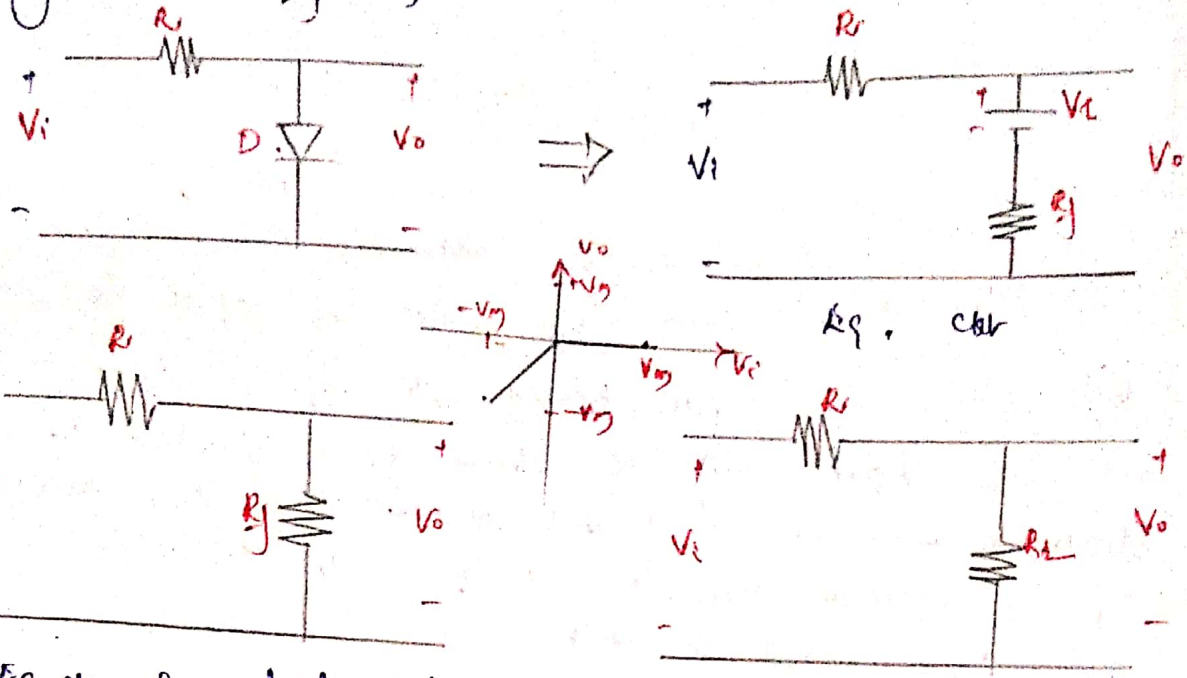


In the double clipping ckt shown clipping occurs at both +ve & -ve voltage levels. When the i/p is greater than +V diode D1 is forward biased and wave form gets clipped. When i/p is less than -V diode D2 is forward biased and wave form gets clipped. Thus in both the cases diode is reverse biased and o/p remains same as input.



Double clipping ckt with both clipping levels are +ve.

* For a Single diode clipper reasonable value of R is the Geometric mean of R_f & R_2.



Eq. ckt when diode ON.

Eq. ckt

Eq. ckt when diode off

$$V_o = \frac{V_i \times R_f}{R_f + R}$$

where $\frac{R_f}{R_f+R}$ is the slope of transfer ckt $= 0$

$\therefore R >> R_f$

$R = kR_f \qquad k = \frac{R}{R_f} \quad \text{---} (1)$

$$V_o = \frac{V_i \times R_2}{R + R_2}$$

$\because \frac{R_2}{R+R_2} = 1$

$R_2 >> R$

$R_2 = k \cdot R$

$k = \frac{R_2}{R} \quad \text{---} (2)$

Comparing eqs (1) & (2)

$$\frac{R}{R_f} = \frac{R_2}{R} \qquad \therefore R^2 = R_f R_2$$

$$R = \sqrt{R_f R_2}$$

Geometric mean of N numbers is the N^{th} root of Product of Given N number

Reasonable value of R would be the Geometric mean of forward resistance R_f and reverse resistance R_2.

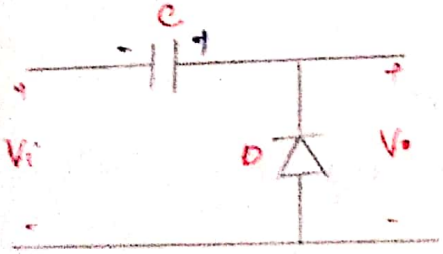
CLAMPER CIRCUITS:

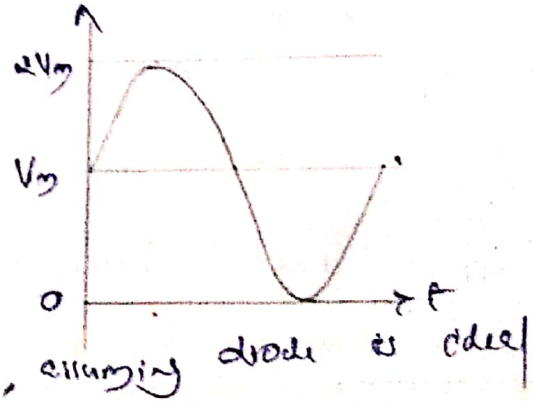
The clamping network is one which will clamp a signal to a different dc level. The network must have a capacitor, diode and a resistive element but it can also employ an independent dc supply to introduce an additional shift. (2)

The following steps may be helpful when analysing clamping networks.

* Start the analysis of clamping network by considering that part of input signal that will forward bias the diode.
* During the period that the diode is ON, capacitor will charge instantaneously to a voltage level determined by the network.
* During the period when diode is off, capacitor will hold on to its established voltage level
* Keep in mind the general rule that total voltage across a load i/p must match the across of input signal.

Positive clamper





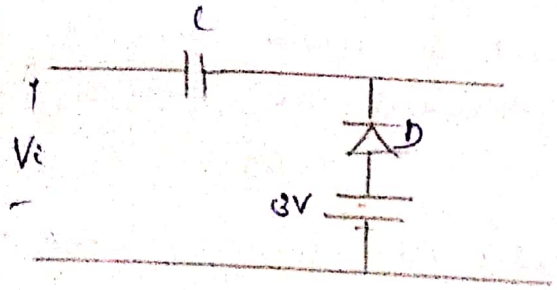
+ve clamping ckt, assuming diode is ideal

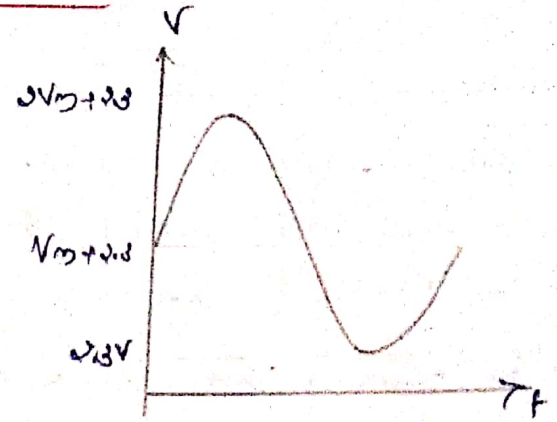
During -ve half cycle of input sine wave, diode conducts and capacitor charges to Vm with +ve polarity at right side of capacitor. During +ve half cycle, the capacitor cannot discharge since diode does not conduct. Thus capacitor acts as a dc source of Vm volts connected in series with signal source. The o/p voltage can be expressed as

$V_{out} = V_{in} + V_m$ since

Positive clamping with Bias

+ve clamping at +ve voltage



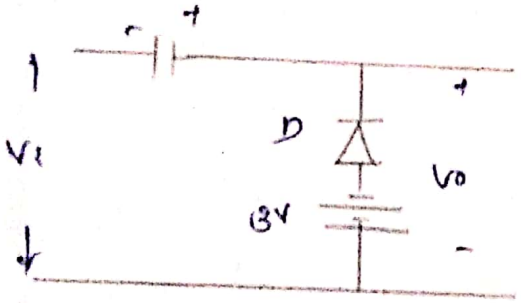


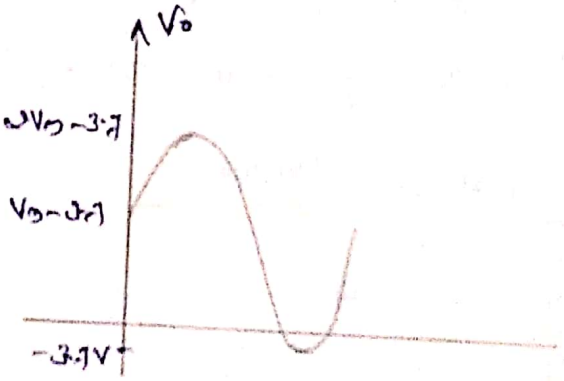
During first -ve half cycle of input sine wave capacitor charges through diode and stable $(V_m + 0.3)$ volts with +ve polarity of capacitor at its right side.

In +ve half cycle this voltage is added with input voltage & gets at o/p.

$$V_o = (V_m + 0.3) + V_m \sin\omega t$$

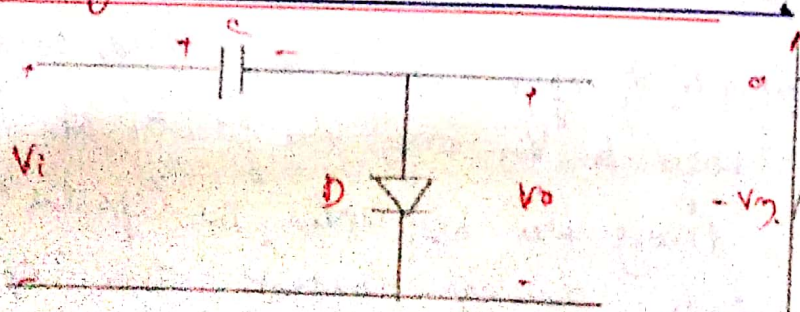
The o/p is clamped at +0.3V.

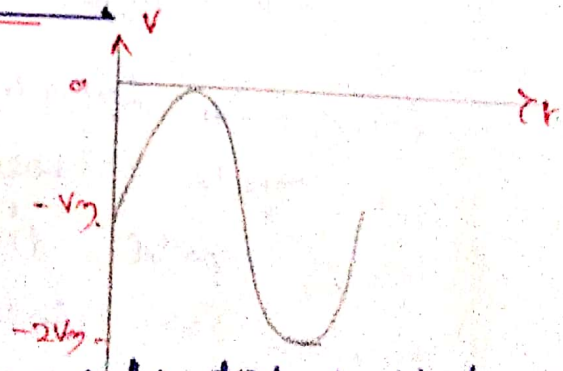




Positive clamping circuit shown clamps at -ve voltage.

Negative clamping Circuits





Negative clamping ckt assuming the diode is ideal.

During first +ve half cycle of input sine wave the diode conducts and capacitor charges to V_m with polarity as shown.

: VOLTAGE MULTIPLIER CIRCUITS

Voltage multiplier is a circuit that produces a dc voltage equal to multiple of the peak input voltage. It consists of two or more peak detectors or rectifiers. Voltage multipliers - some applications in ckts where high voltage with low current is required such as picture tube TV receivers, Oscilloscopes etc.

A voltage multiplier is an electrical ckt that converts ac electrical power from a low voltage to a higher dc voltage by means of capacitors and diodes combined into a network.

Depending on o/p voltage multipliers can be

* Voltage doublers
* Voltage Tripplers
* Voltage Quadrupler.

: VOLTAGE DOUBLERS:

A voltage doubler produces a dc voltage almost twice the peak value of input ac voltage. Voltage doubler can be of two types

⇒ Half wave voltage Doublers

⇒ Full wave voltage doublers.

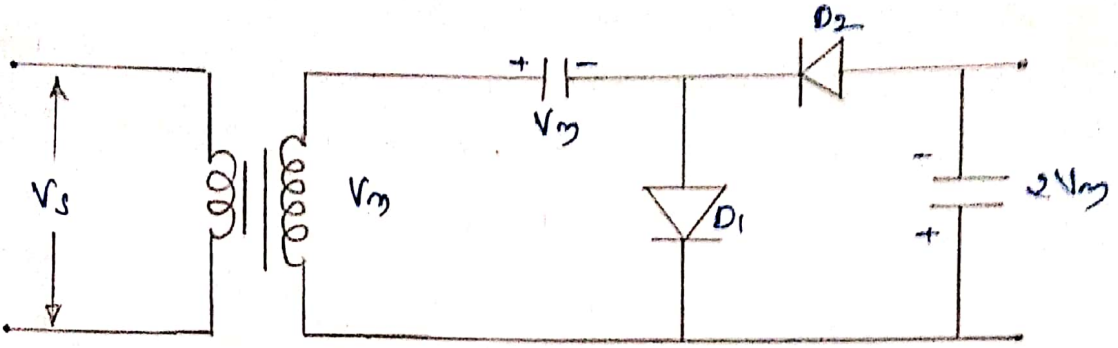
Half wave Voltage Doubler:

Figure shows ckt for HW voltage doubler. During the half cycle of 2^{o} voltage, D_1 conducts and D_2 is cut off. Now capacitor C_1 charges to peak rectified voltage V_m, with

polarity shown in figure. During -ve half cycle the 2° voltage comes in series with voltage across capacitor C_1. Thus C_2 will try to charge towards $2V_m$. Since diode D_2 acts as short during -ve half cycle are see that the voltages around the outside loop.

$$-V_m - V_{C1} + V_{C2} = 0 \quad \text{or} \quad -V_m - V_m + V_{C2} = 0.$$

$$V_{C2} = 2V_m.$$



H.W Voltage Doubler

In figure capacitor C will discharge during -ve half cycle again in the half cycle, it starts charging. Thus the HW voltage doubler supplies the voltage to the load in one half cycles.

Full wave Voltage Doubler

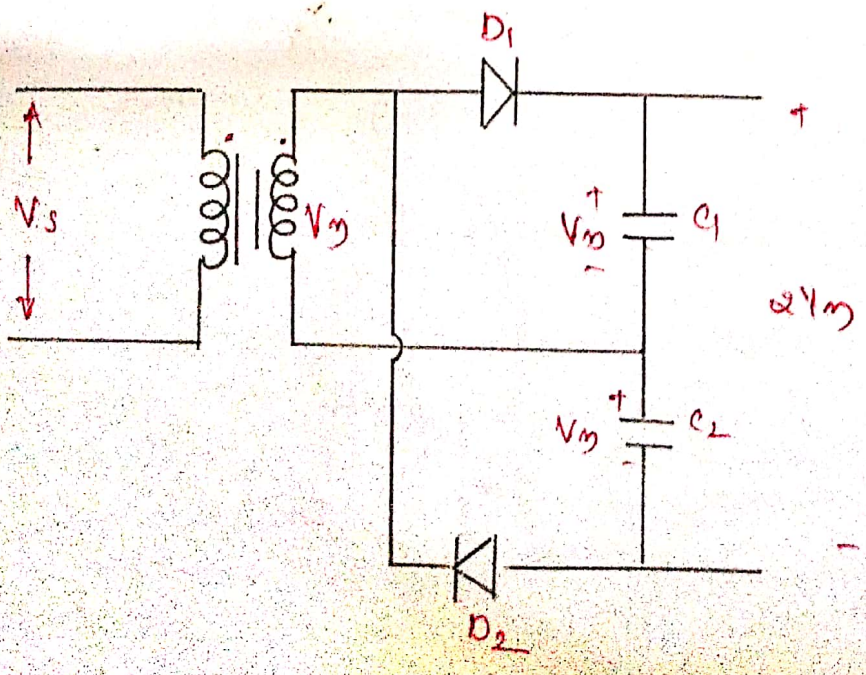
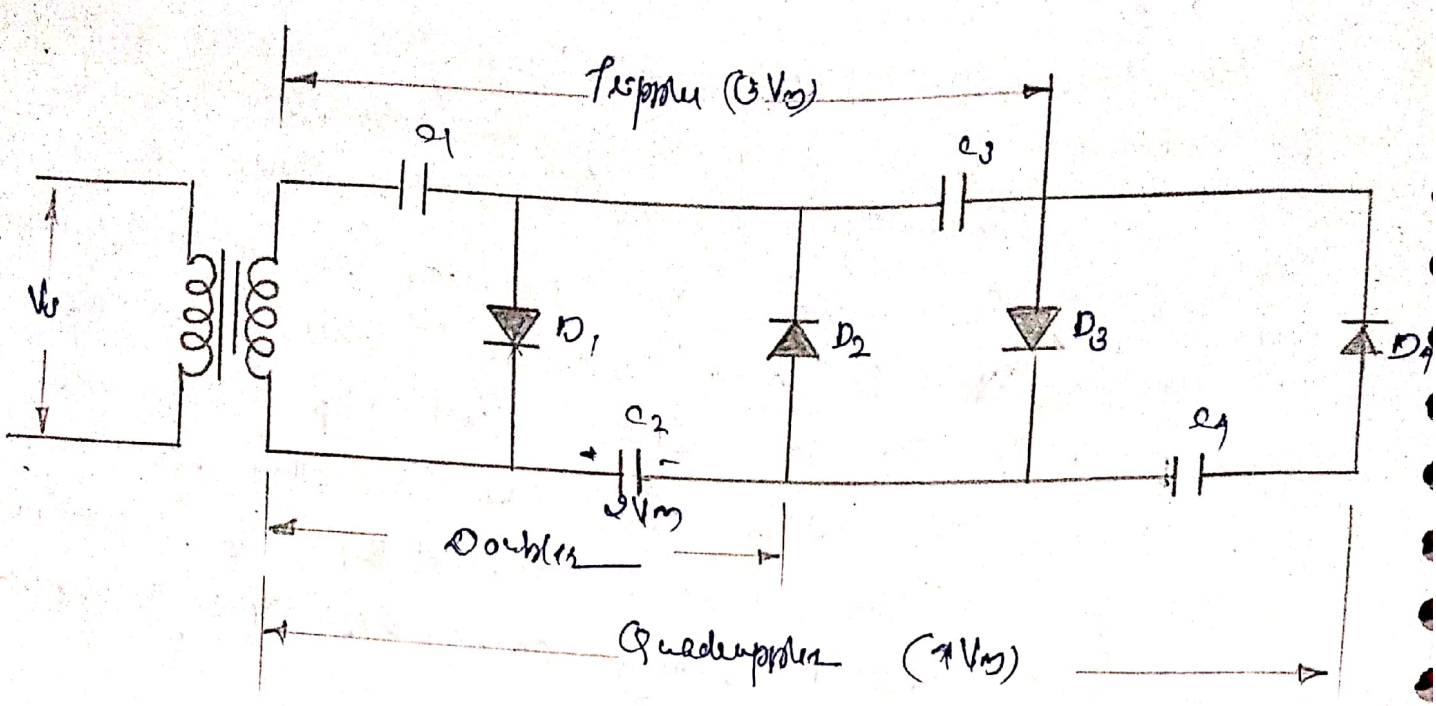


Figure shows FWB voltage regulator. During the +ve half cycle of I/P voltage diode D_1 conducts charging C_1 to peak voltage V_m. At this time D_2 is non-conducting. During -ve half cycle D_2 conducts charging C_2 to V_m. With polarity as marked, while diode D_1 non-conducting. Since both capacitors C_1 & C_2 are in series, final o/p voltage is approximately $2V_m$. This ckt is called full wave voltage doubler because one of the o/p capacitor is being charged during each half cycle of input voltage.

(9)

Voltage Tripler / Quadrupler

Voltage tripler/quadrupler develops a dc voltage equal to three/four times the input ac voltage. Figure shows voltage tripler/quadrupler ckt. On an occurrence of half wave voltage doubler. During +ve half cycle, D_1 conducts, charging C_1 to V_m. During -ve half cycle, diode D_2 conducts charging the capacitor C_2 to $2V_m$. During 2nd +ve half cycle diode D_3 conducts in addition to D_1. charging capacitor C_3 and voltage across capacitor C_2 charges C_3 to same value $2V_m$. On the 2nd negative half cycle diode D_2 & D_4 conducts and capacitor C_4 charges C_4 to $2V_m$. Thus the voltage across C_2 is $2V_m$ across C_1 and C_3 is $3V_m$ and across C_2 & C_4 is $4V_m$.

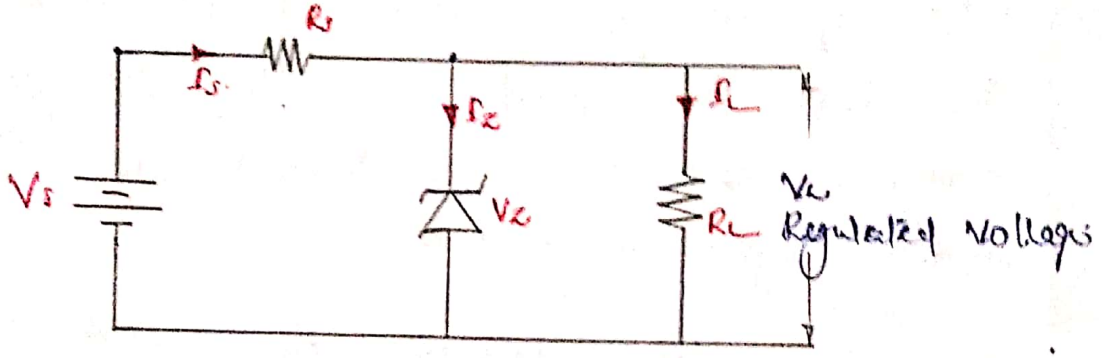

Tripler (3Vm)
C1
C3
Vs
D1
D2
D3
C2
2Vm
C4
Doubler
Quadrupler (4Vm)

MODULE 2

MODULE 5
REGULATED POWER SUPPLIES:

Zener Voltage Regulator: (12)

Zener diode voltage regulator is a shunt regulator because zener is connected in parallel with load. The resistance R_s is used to limit current in the ckt. Regulated op voltage is obtained across load R_L



$V_s = I_s R_s + V_z$ ---(1); $I_s = \frac{V_s - V_z}{R_s}$ ---(2)

load voltage $V_L = V_z$.

$I_s = I_z + I_L$ ---(3)

$I_z = I_s - I_L$

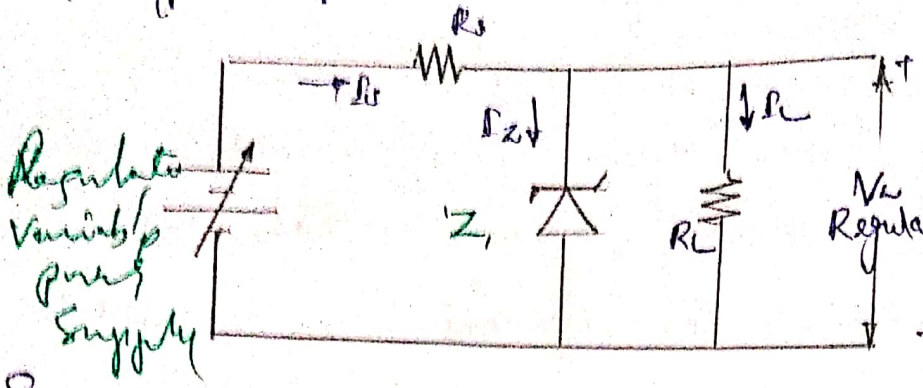
From eqn (2) $\Rightarrow$ $R_s = \frac{V_s - V_o}{I_z + I_L}$

$R_{s\,max} = \frac{V_{s\,max} - V_o}{I_{L\,min} + I_{z\,max}}$

$R_{s\,min} = \frac{V_{s\,max} - V_o}{I_{L\,max} + I_{z\,min}}$

* Line Regulation

In this case load resistance R_L is kept constant and i/p voltage V_s is varied.



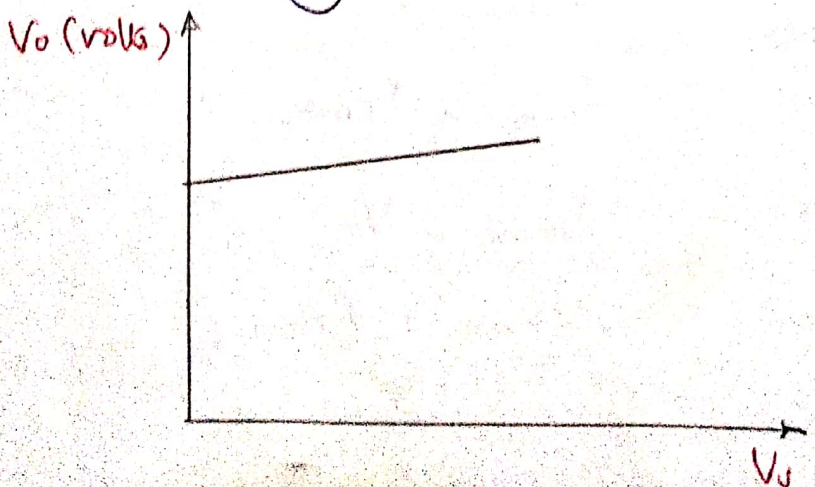
Since $I_s = I_z + I_L$

when o/p voltage increases I_s also increases. This increased current will flow through the zener with out affecting load current I_L. Hence keeping load voltage V_L constant.

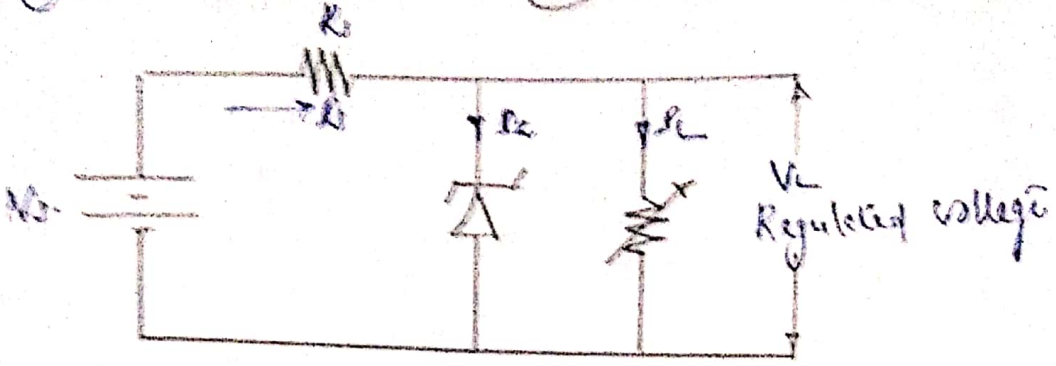
when i/p voltage decreases i/p current also decreases. Due to this current through zener decreases & also the voltage drop across series resistor decreases. Hence load voltage & load current remain constant.

- Line regulation Graph is plotted between i/p voltage & o/p voltage

Percentage regulation = $\frac{\Delta V_o}{\Delta V_s} \times 100$.



* Load Regulation



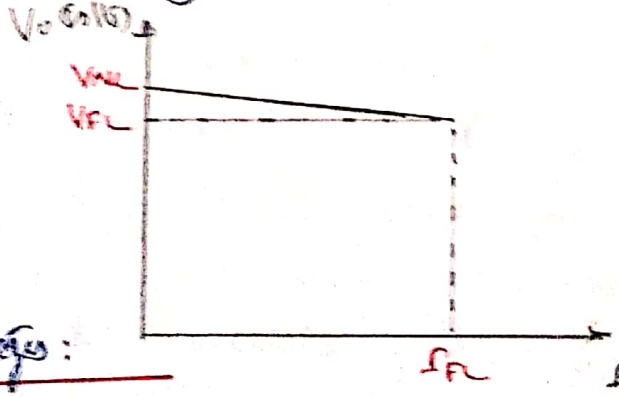
When V_s is kept fixed & R_L is varied.

When R_L decreases load current increases. This causes R_s & voltage across R_s to increase. $\therefore$ V_L is const.

When R_L increases load current decreases. Due to this zener current increases. This again keeps the value of i/p current & voltage drop across R_s as const. $\therefore$ o/p voltage remain const.

Load Regulation Graph is plotted with load current on x axis & o/p voltage on y axis.

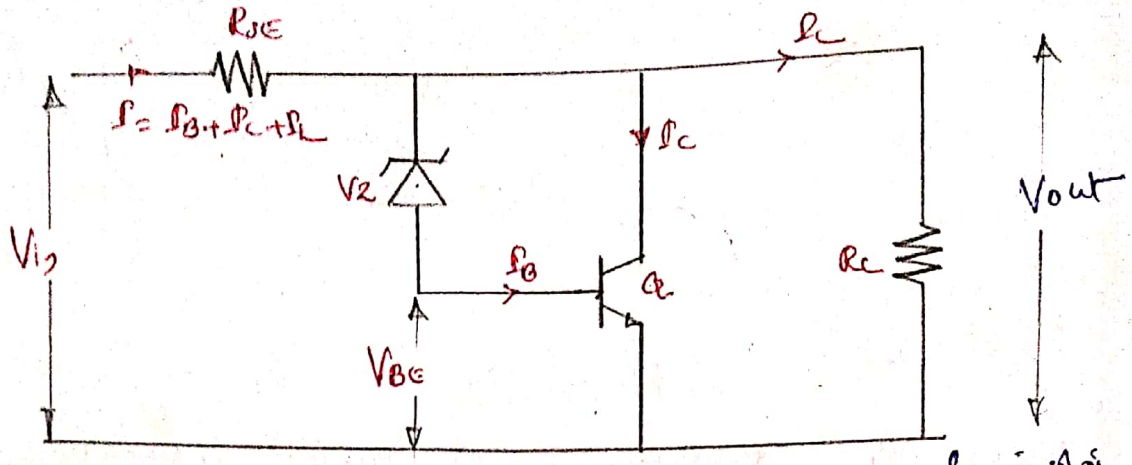
$$\text{Percentage regulation} = \frac{V_{NL} - V_{FL}}{V_{NL}} \times 100$$



Disadvantages:

* It is a fixed voltage regulator & cannot be made adjustable.
* Large power gets dissipated in series resistor R_s
* Corresponding to large changes in load current there will be large changes in zener current. This results in large power wastage.

: Shunt Voltage Regulator Using Transistors:



A shunt voltage regulator using npn transistor & zener diode is shown. R_{SE} is connected in series with input voltage source and the voltage across load is fixed by zener diode and transistor base-emitter voltage V_{BE}

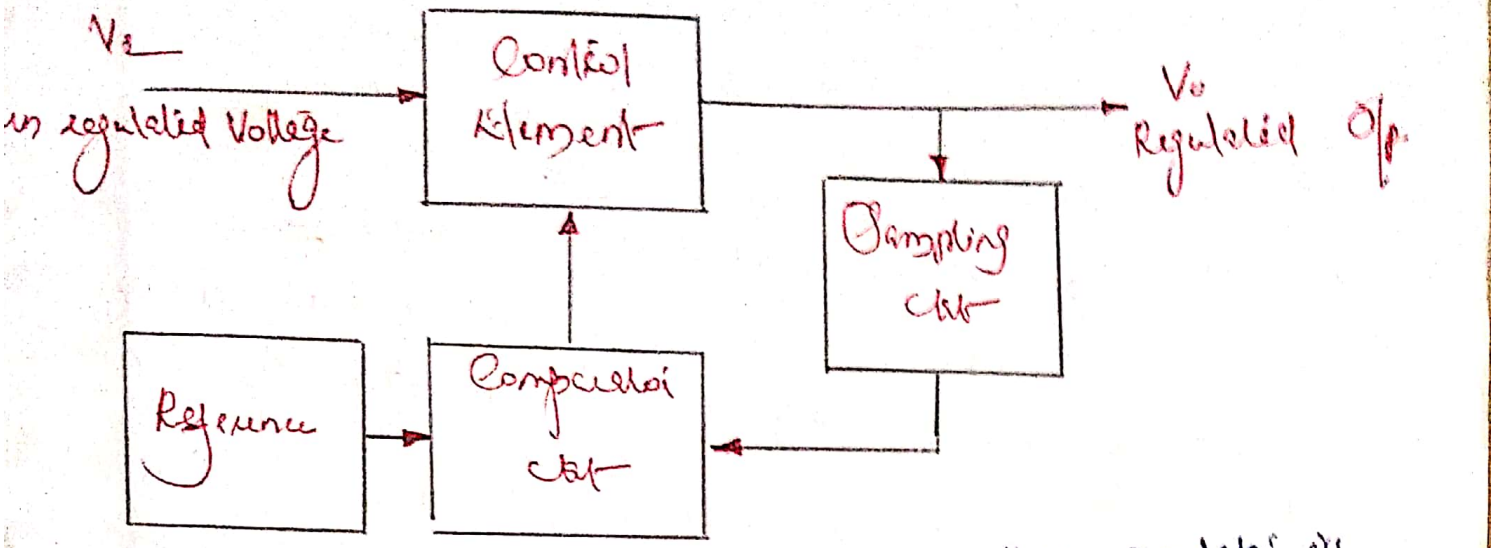
$$V_o = V_Z + V_{BE} = V_{in} - I.R_{SE}$$

Since both V_Z & V_{BE} remain nearly constant V_{out} remains constant.

If input voltage increases I will increase and increased base current I_B results in increased collector current I_C keeping I_L constant and there by V_{out} const. Reverse happens when supply voltage decreases

when R_L decreases I_L increases and this increased I_L is supplied by decrease in I_B and collector current I_C. $\therefore$ I remains const. $\therefore$ V_R is constant and $\therefore$ Vout is also constant Since V_S is constant. Reverse happens when load R_L increases.

Series Voltage Regulator:



The basic connection of Series voltage regulator is shown. The series element controls the amount of input voltage that gets to o/p. The o/p voltage is sampled by a ckt that provides feedback voltage to be compared to reference voltage.

* If o/p voltage increases, the comparator ckt provides a control signal to cause series control element to decrease the amount of o/p voltage, thus by maintaining o/p voltage.
* If the o/p voltage decreases, the comparator ckt provides a control signal to cause series control element to increase the amount of o/p voltage.

Emitter follower Series pass Regulator:

The power transistor used in this configuration is known as pass transistor. Because of the current amplifying property of transistor

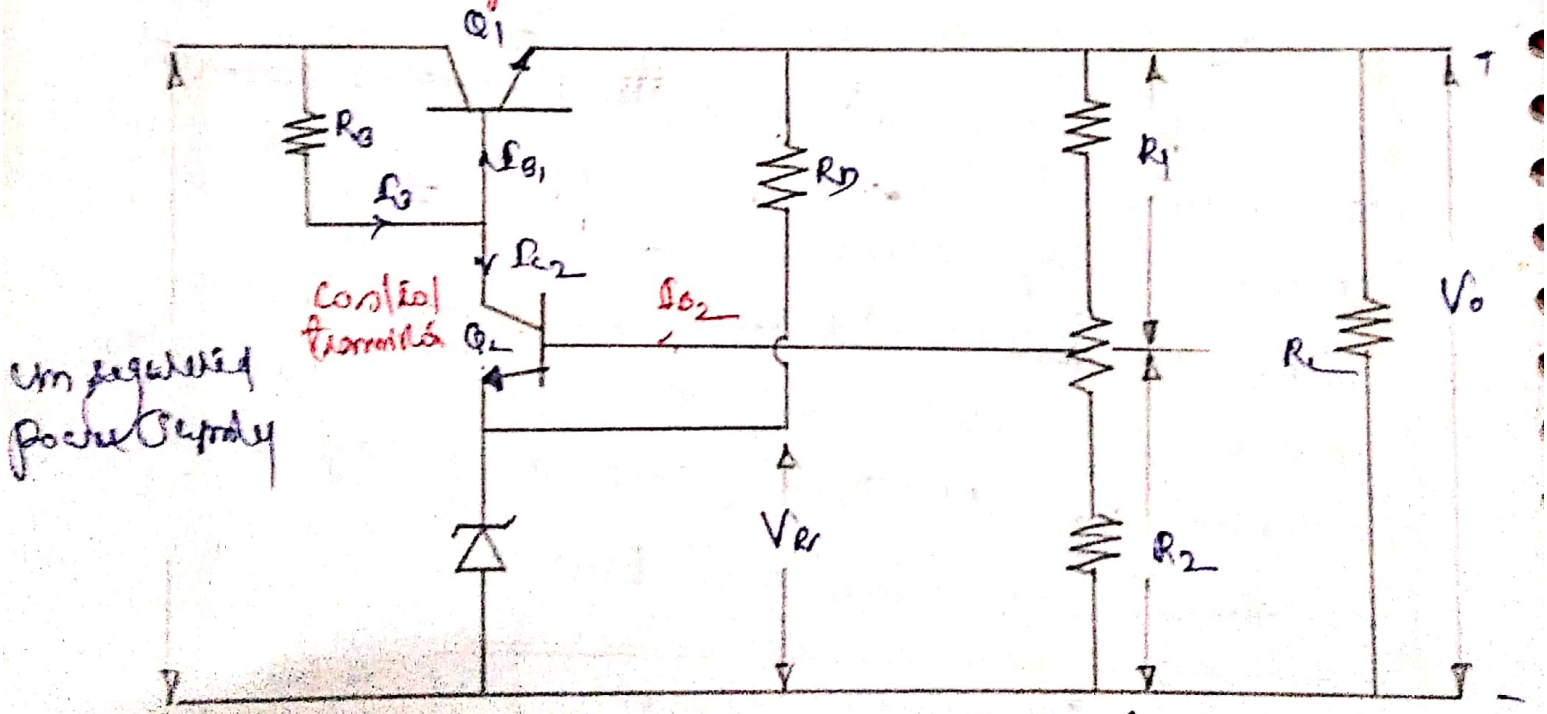
the current in zener diode is small. Hence there is little drop across diode and zener approximates an ideal constant voltage source

Transistor Q_1 is the series control element and zener diode provides reference voltage. The regulating operation is as follows.

* If o/p voltage decreases, increased base emitter voltage causes transistor Q_1 to conduct more there by raising o/p voltage - maintaining o/p constant
* If the o/p voltage increases, the decreased base emitter voltage causes Q_1 to conduct less there by reducing o/p voltage. - maintaining o/p constant.

Series pass transistor Voltage Regulator.

Series pass transistor



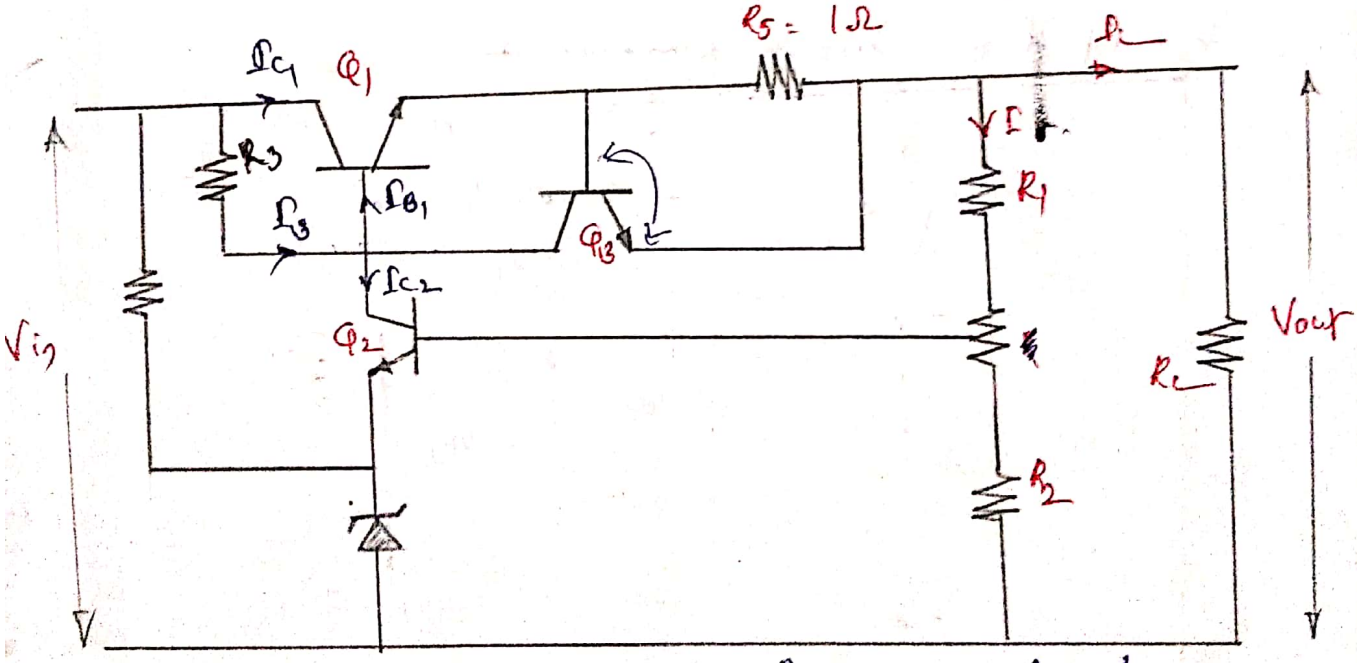
Here the control voltage transistor Q_2's emitter terminal is connected to -ve terminal of supply through zener diode

The voltage regulator employs the principle of negative feedback to hold o/p voltage almost constant.

Q_1 is the pass transistor because all load current flows through it.

If the o/p voltage increases, the voltage across R_2 is also increases. This causes increase in base bias of Q_2; as a result I_{B_2} and I_{C_2} increases. Assuming I_B constant, I_{B_1} decreases. Decrease in base current of transistor Q_1 causes increase in collector-emitter resistance of Q_1. This causes increase in V_{CE_1} and offsetting the increase in o/p voltage. Thus o/p voltage remains constant. Reverse happens when the o/p voltage decreases.

* Controlled transistor Series Regulator with Overload & Short Circuit protection. *



If the load resistance R_L is reduced or load terminals are shorted accidently, a very large current will flow in the ckt; it may destroy the pass transistor Q_1.

- To avoid this situation current limiting ckt is added to series regulator.

The current limiting ckt consists of transistor Q_3 and resistor R_5 connected b/w base and emitter of Q_3.

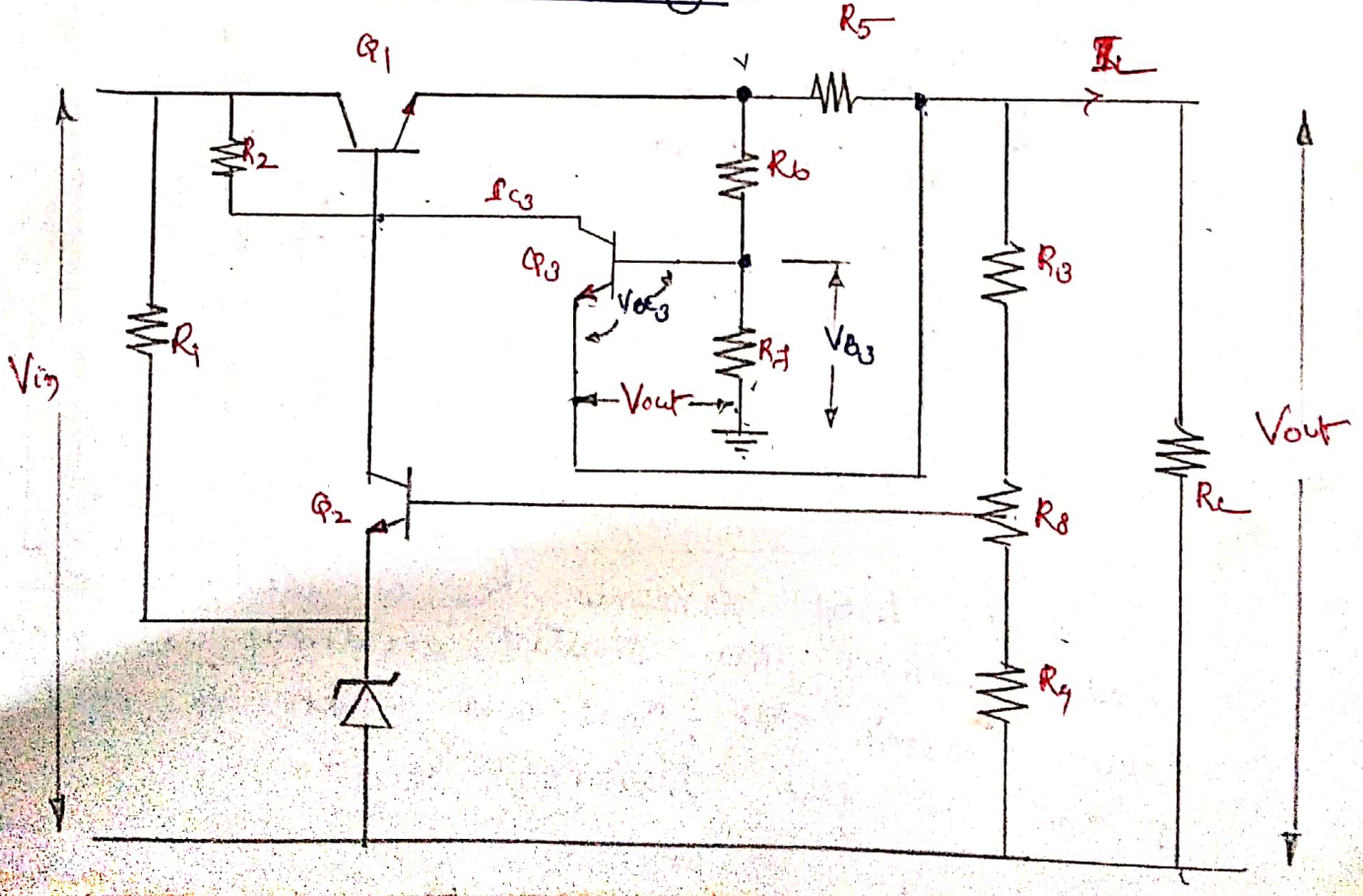
With normal load current, Q_3 remains off because the voltage drop across R_5 is small. Under this condition ckt works normally.

With excessive load current [exceeding $\frac{0.6}{1} = 0.$ or 600mA] the voltage drop across R_5 is enough to turn ON transistor Q_3. The collector current of Q_3 flows through R_3 decreasing base voltage of Q_1. This results in reduction of conduction level of Q_1. Thus further increase in load current is prevented.

Power dissipation across pass transistor

$$P_V = (V_{in} - V_{BE}) I_{SC}$$

* Fold back Current limiting: *



In short circuit protection Rsc is large amount of power dissipating in circuit then transistor Q_1 enter the regulation region from saturation.

In foldback circuit base of Q_3 is biased by voltage divider n/w of R_5 & R_4 the load current I_L flows through R_5 causing drop across it. Thus voltage of $(I_L R_5 + V_{out})$ acts across (R_4 & R_4) n/w. The voltage applied to base of Q_3 is equal to the voltage drop across R_4 and is

$$V_{B3} = \frac{R_4}{R_5 + R_4}\left[I_L R_5 + V_{out}\right] = k\left[I_L R_5 + V_{out}\right]$$

$$V_{BE3} = V_{B3} - V_{out} = k\left[I_L R_5 + V_{out}\right] - V_{out}$$

$$V_{BE3} = k I_L R_5 + (k-1)V_{out}$$

Now if load resistance decrease, load current I_L will increase causing drop $I_L R_5$ to increase. This makes V_{B3} to increase & $\therefore$ V_{BE3} will also increase and Q_3 will conduct more. The increased collector current I_{C3} of transistor Q_3 flows through R_3 decreasing base bias of Q_1. This results in reduction of conduction level of Q_1. Thus further increase in load current is prevented.

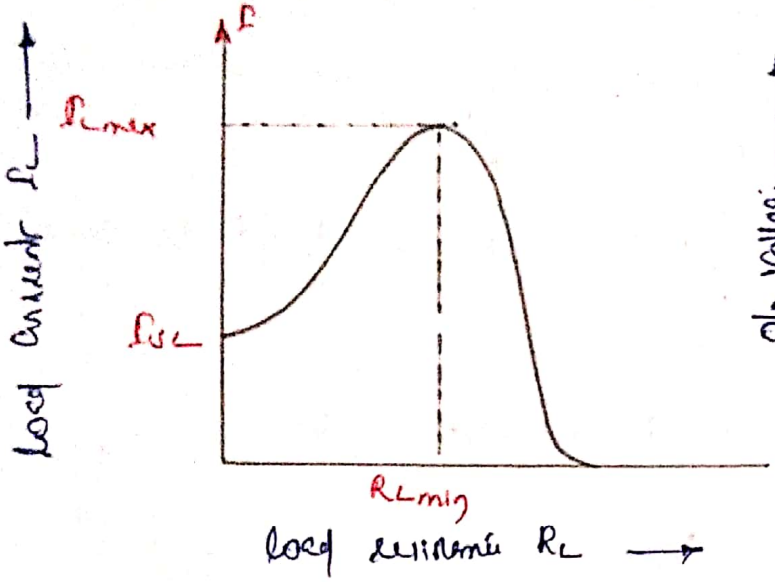
Due to reduction in load resistance V_{BE3} increases to a level at which Q_3 gets saturated. Now collector current I_{C3} becomes constant. Any further decrease in R_L will have no effect on I_{C3}. The corresponding load current I_{max} is

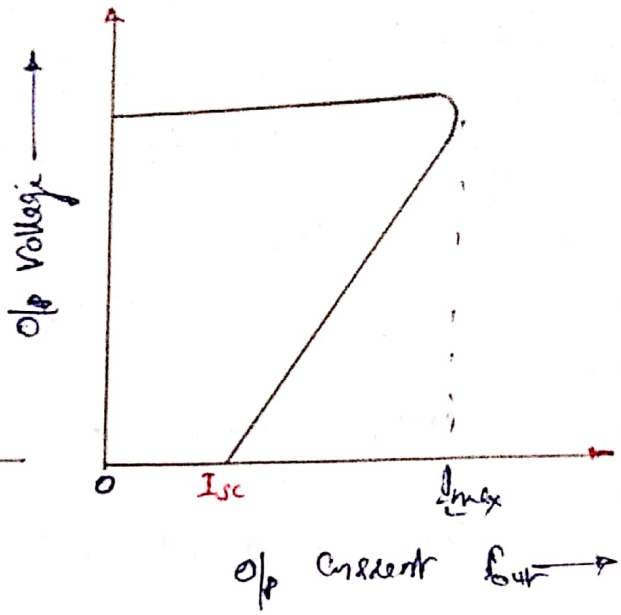
$$I_{max} = \frac{V_{BE3}}{k R_5} + \frac{(k-1)V_{out}}{k R_5}$$

Beyond this point V_{BE_3} drops due to saturation with load resistance $R_L = 0$ $V_{out} = 0$.

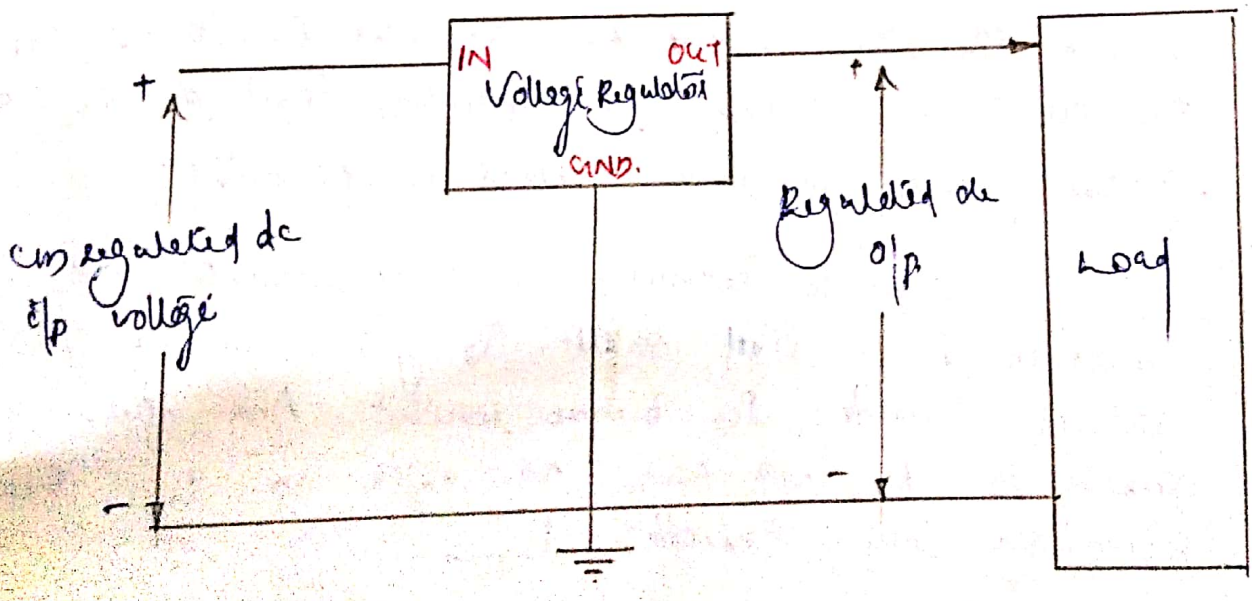
$$\therefore I_{SC} = \frac{V_{BE_3}}{R R_5}$$

Should load current I_{SC} is much less than $I_{L\,max}$ providing -fold back current limiting.





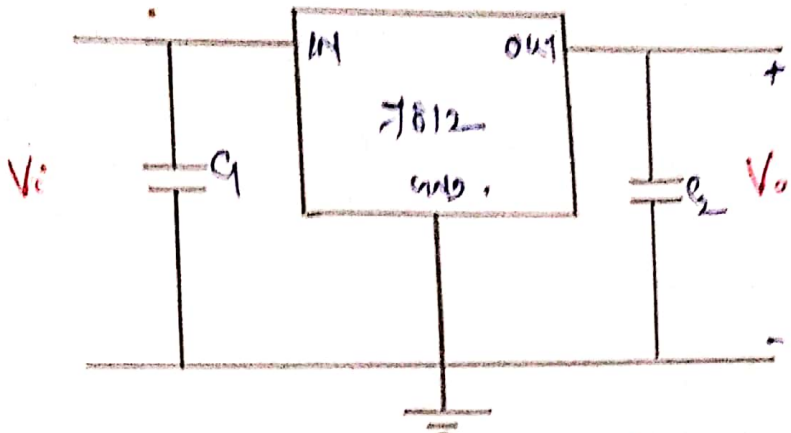
: Three Terminal Voltage Regulator:



Block representation of 3-Terminal voltage regulator.

Fixed voltage regulator has an unregulated dc i/p voltage applied to one i/p terminal, regulated o/p V_o from 3rd terminal and 2nd terminal connected to ground.

Fixed +ve Voltage Regulators: [78xx Series] (15)



Series 78 regulators provide fixed regulated voltages from 5V to 24V. In 78XX unregulated i/p Vi is ~~applied~~ filtered by capacitor C and connected to IC's IN terminal. IC's out terminal provides regulated +12V. 3rd terminal is connected to ground.

IC part	O/p Voltage V_o
7805	+5
7806	+6
7808	+8
7810	+10
7812	+12
7815	+15
7818	+18
7824	+24

+ve Voltage Regulators in 78xx Series.

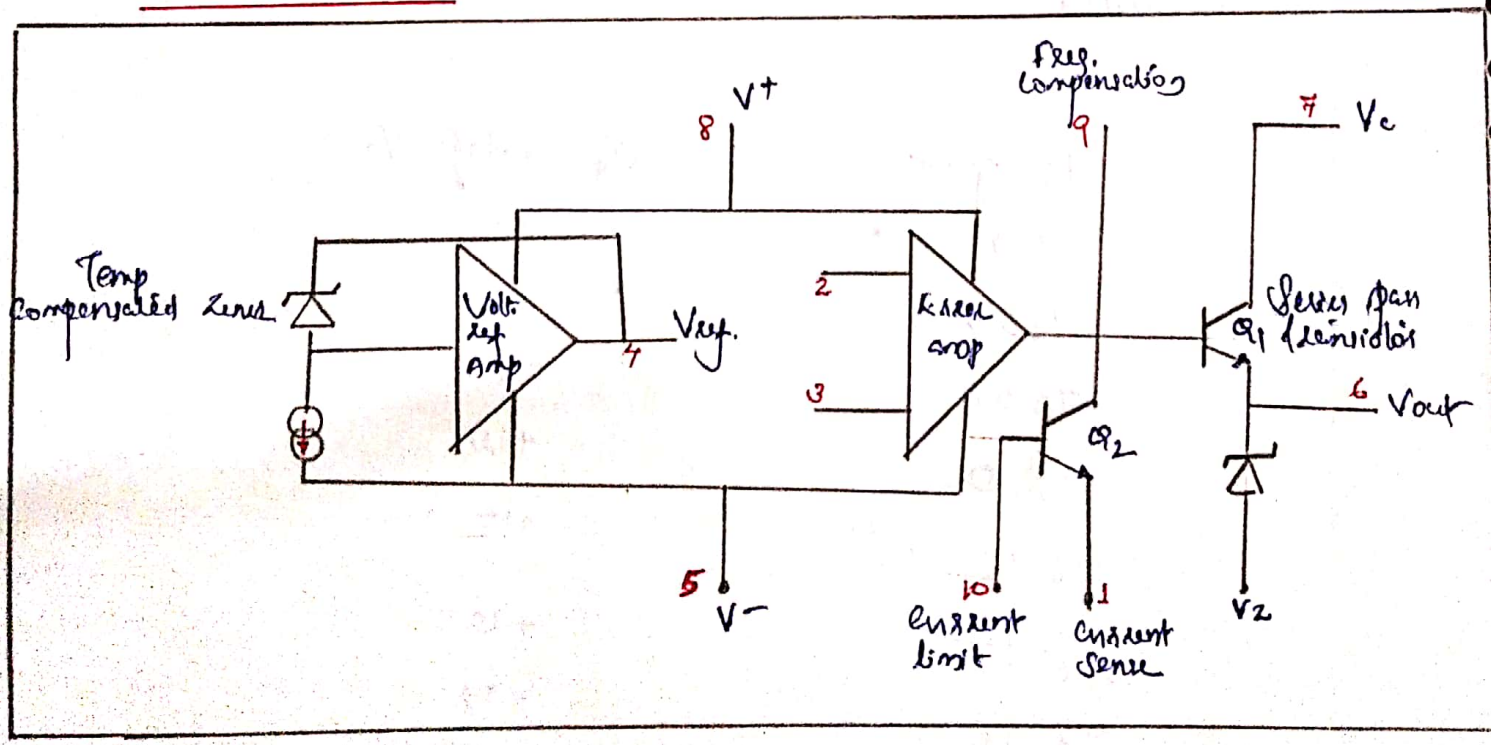
Fixed -ve Voltage Regulators: [79xx Series]

The Series 79xx provides -ve Voltages (regulated). It also provide regulated o/p from -5V to -24V.

Ic part	O/p voltage V
7905	-5
7906	-6
7908	-8
7909	-9
7912	-12
7915	-15
7918	-18
7924	-24

Adjustable Voltage Regulators:

Ic 723



Internal BD of 723

The internal working can be explained by dividing it into two blocks. Reference Voltage Generator and Error amplifier

In the reference voltage generator a Zener diode is being compelled to operate at a fixed point by a constant current source which comes along with an amplifier to generate a constant voltage of 7.15V at Vref pin of I.C.

Error amplifier section consisting of error amp. series pass transistor and a current limiting transistor. Error amp can be used to compare the o/p voltage applied at inverting input terminal and Vref applied at Non-inverting input terminal. Conduction of transistor Q_1 is controlled by error signal. & Q_1 controls o/p voltage.

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The functioning of the above blocks can be explained with the help of a simplified functional block diagram of IC 723 as shown in the Fig. 7.44.

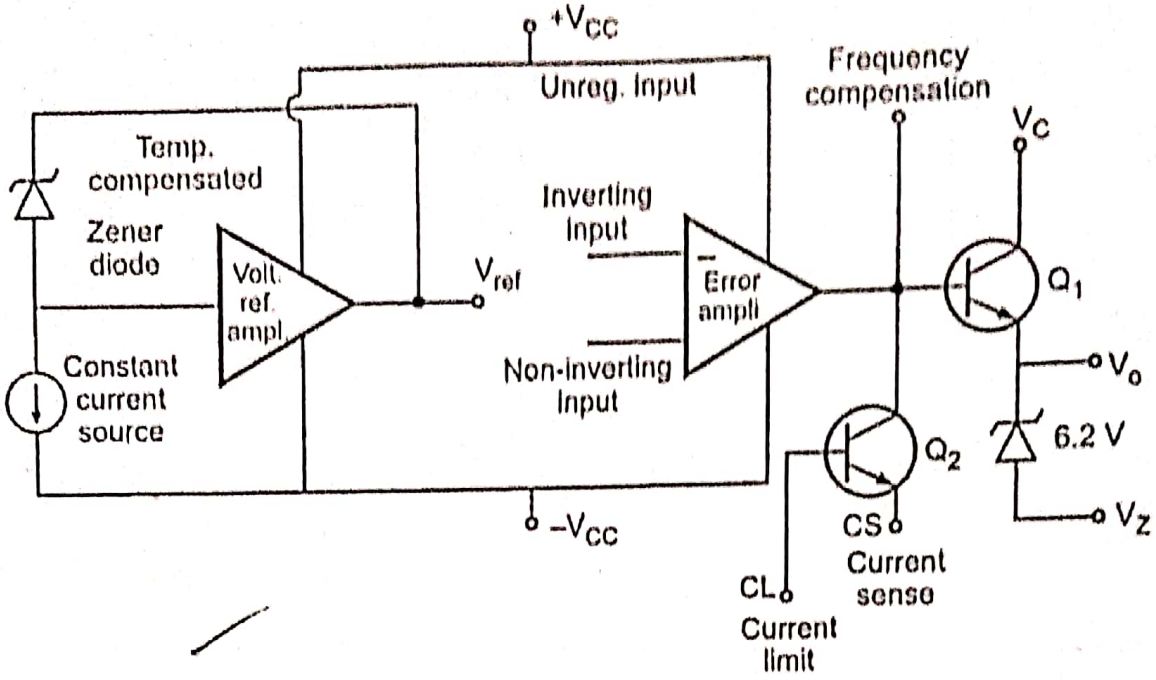


Fig. 7.44 Functional block diagram

Temperature compensated zener diode, constant current source and reference amplifier constitutes the reference element.

Key Point: *In order to get a fixed voltage from zener diode, the constant current source forces the zener to operate at a fixed point.*

Output voltage is compared with this temperature compensated reference potential of the order of 7 volts. For this, V_{ref} is connected to the non-inverting input of the error amplifier.

This error amplifier is high gain differential amplifier. It's inverting input is connected to the either whole regulated output voltage or part of that from outside. For later case a potential divider of two scaling resistors is used. Scaling resistors help in getting multiplied reference voltage or scaled up reference voltage.

Error amplifier controls the series pass transistor Q_1, which acts as variable resistor. The series pass transistor is a small power transistor having about 800 mW dissipation. The unregulated power supply source (< 36V d.c.) is connected to collector of series pass transistor.

Transistor Q_2 acts as current limiter in case of short circuit condition. It senses drop across R_{sc} placed in series with regulated output voltage externally.

The frequency compensation terminal controls the frequency response of the error amplifier. The required roll-off is obtained by connecting a small capacitor of 100 pF between frequency compensation and inverting input terminals.

The internal structure can be represented in more simplified form as shown in the Fig. 7.45

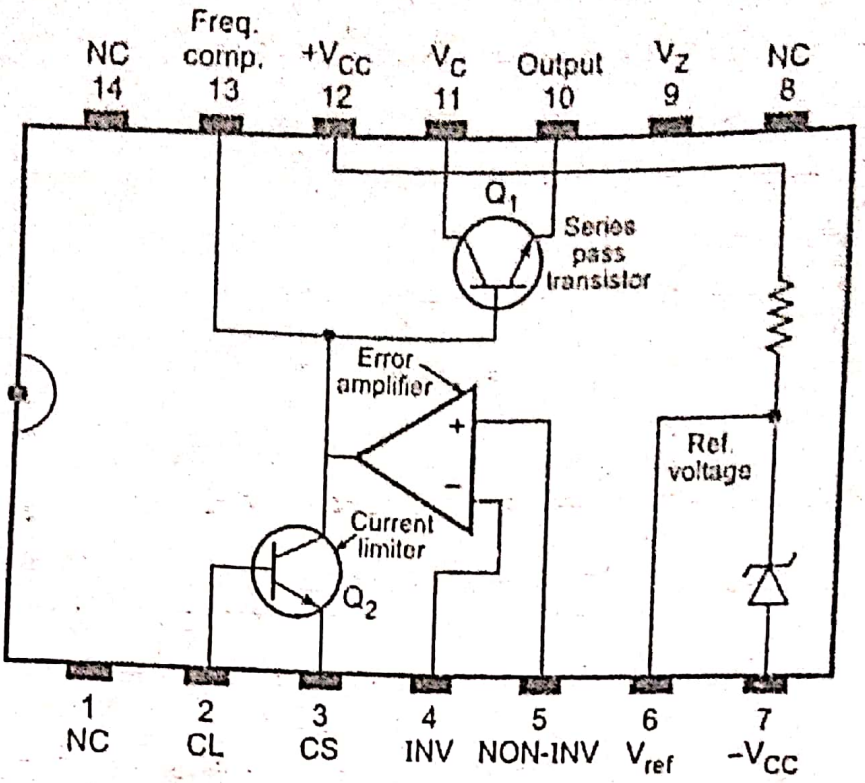


Fig. 7.45 Simplified internal structure of IC 723

Both noninverting and inverting terminals of the error amplifier are available on outside pins of IC 723. Due to this, device becomes versatile and flexible to use. Only restriction is that internal reference voltage is 7 volts and therefore we have to use two different circuits for getting regulated outputs of below 7 volts and above 7 volts.

7.14.3 Specifications of IC Regulator 723

The Table 7.2 gives the electrical specifications of IC 723. In the Table 7.2 some of the specifications are specified depending upon the application area of IC 723. There are two application area namely military grade applications and commercial grade applications, denoted namely by M and C.

Electrical Specifications	
Absolute Maximum Ratings over Operating Free-Air Temperature Range (Unless otherwise Noted)	
Peak voltage from V_{CC+} to V_{CC-} ($t_w \leq 50$ ms)	50 V
Continuous voltage from V_{CC+} to V_{CC-}	40 V
Input-to-output voltage differential	40 V
Differential input voltage to error amplifier	± 5 V
Voltage between noninverting input and V_{CC-}	8 V

Current from V_z	25 mA
Current from $V_{in(+)}$	15 mA
Continuous total dissipation at (or below) 25°C free-air temperature	
J or N package	1000 mW
L package (see Note 1)	800 mW
U package	675 mW
Operating free-air temperature range : µA723M Circuits	–55°C to 125°C
µA723C Circuits	0°C to 150°C
Storage temperature range	–65°C to 150°C
Lead temperature $\frac{1}{16}$ in. form case for 60s, J, L, or U package	300°C
Lead temperature $\frac{1}{16}$ in. form case for 10s, N package	260°C

Note: 1. This rating for the L package requires a heat sink.

Table 7.2

The Table 7.3, gives the safe operating conditions of IC 723. These conditions a provided by the manufacturer.

	Min	Max	Unit
Input voltage, V_i	9.5	40	V
Output voltage, V_o	2	37	V
Input -to-output voltage differential, $V_C - V_o$	3	38	V
Output current, I_o		150	mA

Table 7.3 Recommended operating conditions

7.14.4 Applications of IC 723

The various regular circuits as per the requirement can be achieved using IC723. So of them are discussed below :

7.14.4.1 Basic Low-voltage Regulator (V_o = 2 to 7 volts)

The resistor, R_{sc} is connected between CL and CS pins. The current limit transis remains non-conductive unless drops across R_{sc} is 0.6 V (equal to V_{BE} drop). The value R_{sc} can be found out by following equation

$$R_{sc} = \frac{V_{sense}}{I_{limit}} = \frac{0.6}{I_{limit}}$$

I_{limit} can be selected as 1.2 to 1.5 times the maximum load circuit. Potential divi made up of R_1 and R_2 is connected between V_{ref} and non-inverting terminals.

$$V_{non\text{-}inverting} = V_{ref} \times \frac{R_2}{R_1 + R_2} \quad \ldots (2)$$

As the series pass transistor is working as emitter follower.

$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2} \quad \ldots (3)$$

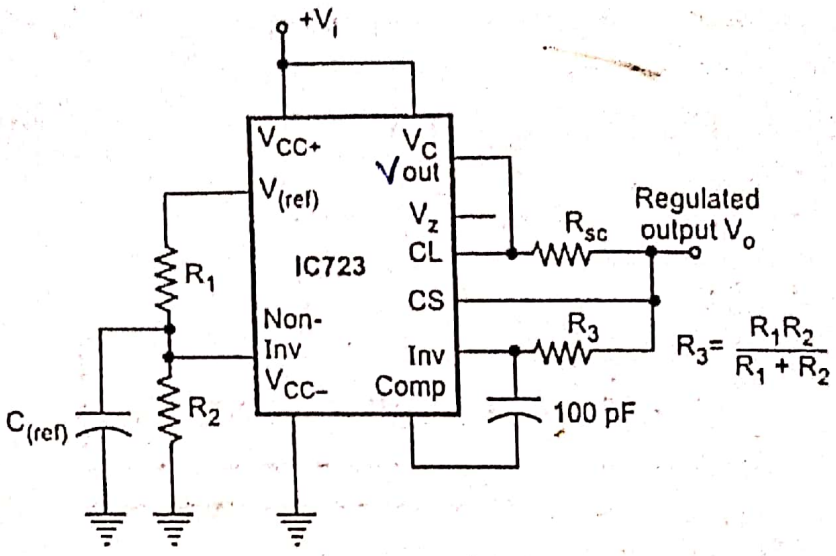


Fig. 7.46 Basic low-voltage regulator

R_1 and R_2 can be between 1 kΩ to 10 kΩ.

$$R_3 = R_1 \parallel R_2 \quad \therefore \boxed{R_3 = \frac{R_1 R_2}{R_1 + R_2}} \quad \ldots (4)$$

Maximum load current can be 150 mA.

7.14.4.2 Low Voltage High Current Regulator

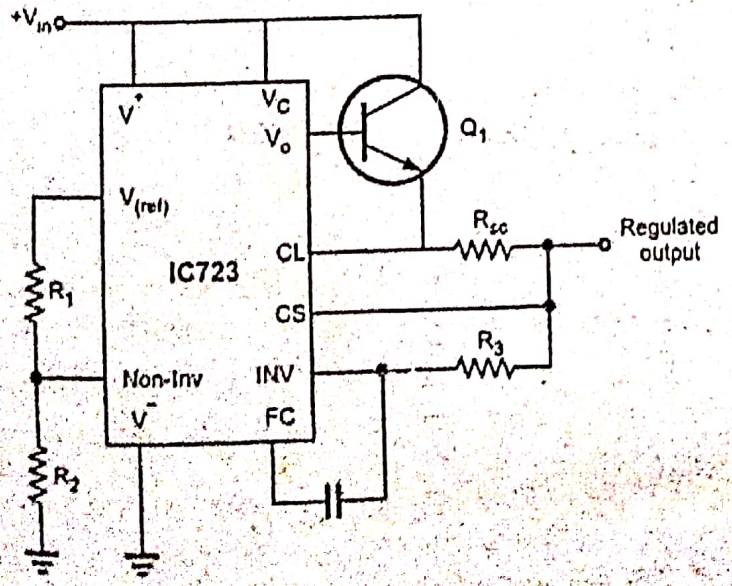


Fig. 7.47

Output voltage from +2 to +7 V and load current can be more than 150 mA. For this one transistor is connected externally, shown as Q_1 in the Fig. 7.47.

The functional equations are similar to that of basic low voltage regulator circuit.

$$\boxed{V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}}$$

$$\boxed{R_{sc} = \frac{0.6}{I_{limit}}}$$

Power dissipation of transistor = $[V_{i(max)} - V_{o(min)}] \times I_{L(max)}$ ... (5)

Power dissipation of IC = $[V_{i(max)} - V_{o(min)}] \times \frac{I_{L(max)}}{h_{fe(min)} \text{ of } Q_1}$ ... (6)

7.14.4.3 Basic Positive High Voltage Regulator

For this type, output voltage varies from +7 V to +37 V and $I_L \leq 150$ mA.

The non-inverting terminal connected to V_{ref} through R_3. Due to this arrangement the error amplifier acts as non-inverting amplifier.

The gain $$A = 1 + \frac{R_1}{R_2}.$$

The output voltage is,

$$V_o = V_{ref}\left(1 + \frac{R_1}{R_2}\right) = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right) \quad \text{... (7)}$$

$$R_{sc} = \frac{0.6}{I_{limit}} = \frac{V_{sense}}{I_{sc}} \quad \text{... (8)}$$

$$R_3 = R_1 \parallel R_2 = \left(\frac{R_1 R_2}{R_1 + R_2}\right) \quad \text{... (9)}$$

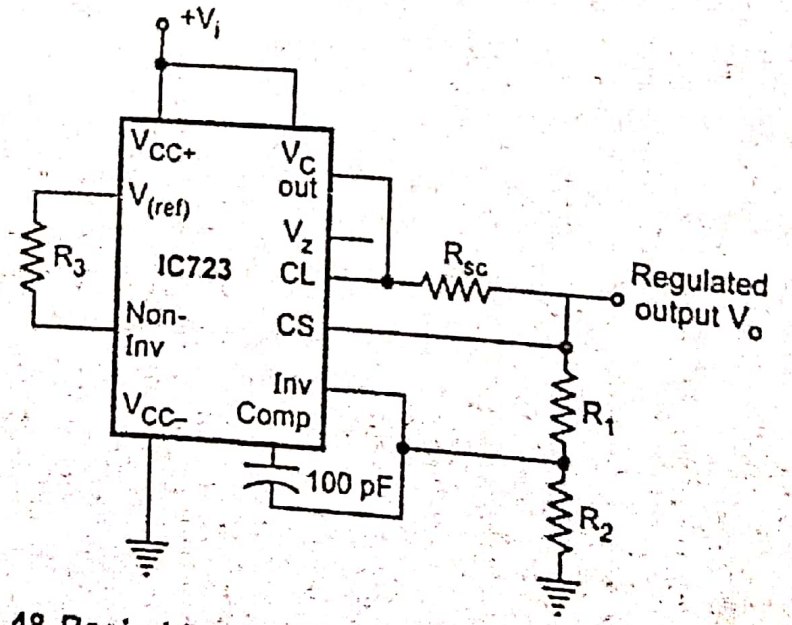


Fig. 7.48 Basic high-voltage regulator (V_o = 7 to 37 volts)

This is also called basic high voltage low current regulator.

7.14.4.4 Positive High Voltage High Current Regulator

For this type, output voltage from +7 V to +37 V and load current I_L > 150 mA. For this a external transistor Q_1 is connected, as shown in the Fig. 7.49.

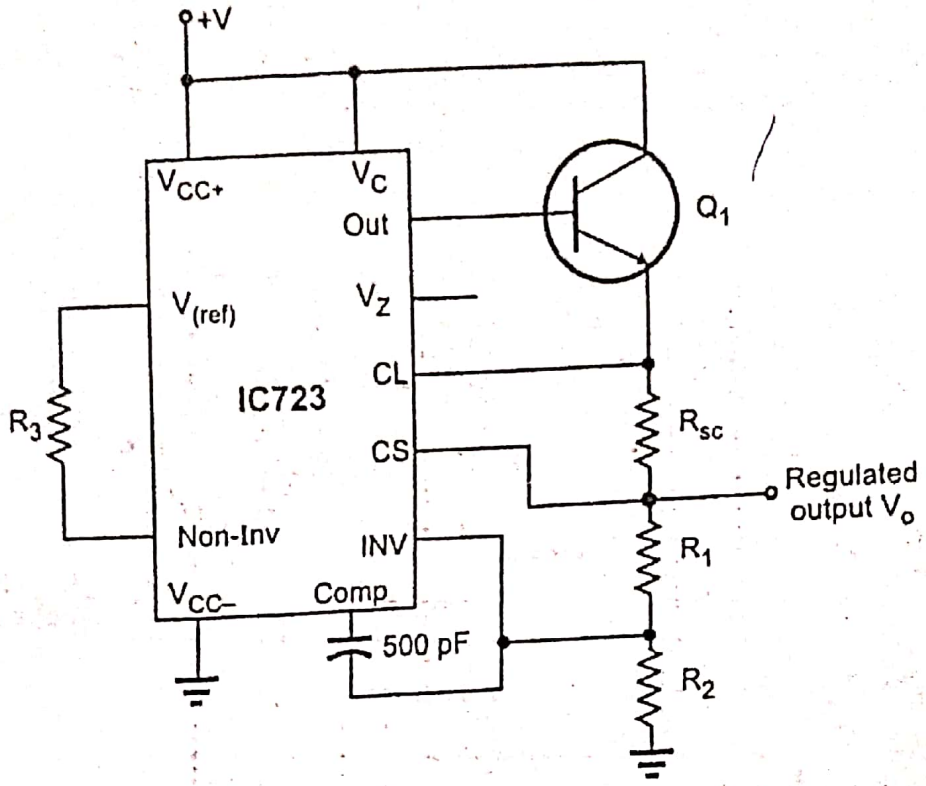


Fig. 7.49 Positive high voltage regulator

For this different expressions are similar to basic high voltage regulator and reproduced for the convenience.

$$V_o = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right)$$

$$R_{sc} = \frac{0.6}{I_{limit}} = \frac{V_{sense}}{I_{sc}}, \quad R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

While the power dissipation of transistor Q_1 and the IC is given by the same expressions as given by the equations (5) and (6).

7.14.4.5 Negative Voltage Regulator

Connections for getting negative voltage regulator are shown in Fig. 7.50. An external PNP transistor, Q_1 is connected. Resistances can be from 1 kΩ to 10 kΩ.

$$R_3 = R_4 \quad \cdots (10)$$

$$V_{out} = \left[\frac{V_{ref}}{2} + \frac{R_1 + R_2}{R_1}\right] \quad \cdots (11)$$

If magnitude of $-V_i$ is less than 9V, connect V_{CC+} and V_C to a positive supply such that V_{CC+} to V_{CC-} is greater than 9V, for proper functioning of the IC.

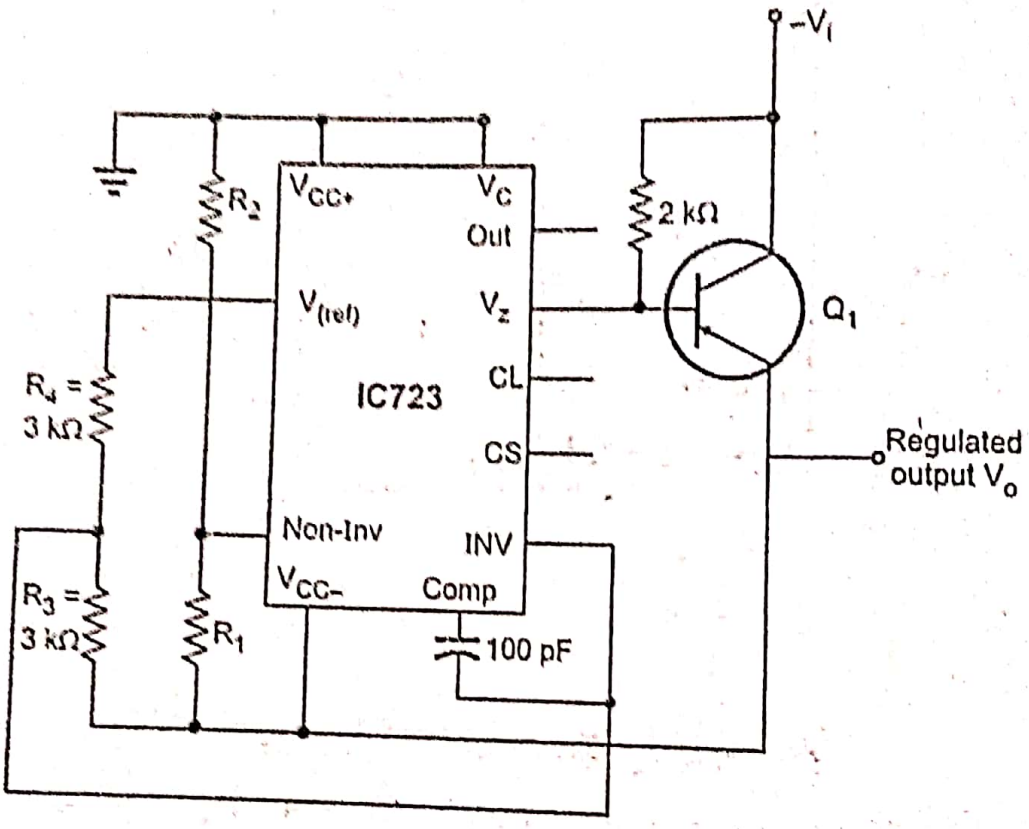


Fig. 7.50 Negative voltage regulator

Example 7.10 : *Design a regulator using IC 723 to meet the following specifications :*

$V_o = 5V$; $I_o = 100\ mA$.

$V_{in} = 15 \pm 20\ \%$

$I_{sc} = 150\ mA$; $V_{sense} = 0.7\ V$.

Solution : The given specifications are

$V_o = 5V$; $I_o = 100$ mA.

$V_{in} = 15 \pm 20\ \%$

$I_{sc} = 150$ mA; $V_{sense} = 0.7$ V.

Now $$R_{sc} = \frac{V_{sense}}{I_{sc}} = \frac{0.7}{150 \times 10^{-3}} = 4.67\ \Omega$$

Neglecting input bias current of an error amplifier we can write,

$$R_1 = \frac{V_{ref} - V_0}{I_D}$$

where I_D = potential divider current = 1 mA

and V_{ref} = 7.15 V for IC 723

$$\therefore \quad R_1 = \frac{7.15 - 5}{1 \times 10^{-3}} = 2.15 \text{ k}\Omega$$

Use 2.2 kΩ standard resistance.

Now $$V_0 = V_{ref} \cdot \frac{R_2}{R_1 + R_2}$$

$$\therefore \quad 5 = 7.15 \cdot \frac{R_2}{(2.2 + R_2)}$$

$$\therefore \quad 2.2 + R_2 = 1.43\, R_2$$

$$\therefore \quad 0.43\, R_2 = 5.11 \text{ k}\Omega$$

Use 5.1 kΩ standard resistor.

$$R_3 = R_1 \| R_2$$

$$= \frac{2.2 \times 5.1}{2.2 + 5.1} = 1.536 \text{ k}\Omega$$

Use 1.5 kΩ (standard) resistor.

The designed regulator is shown in the Fig. 7.51.

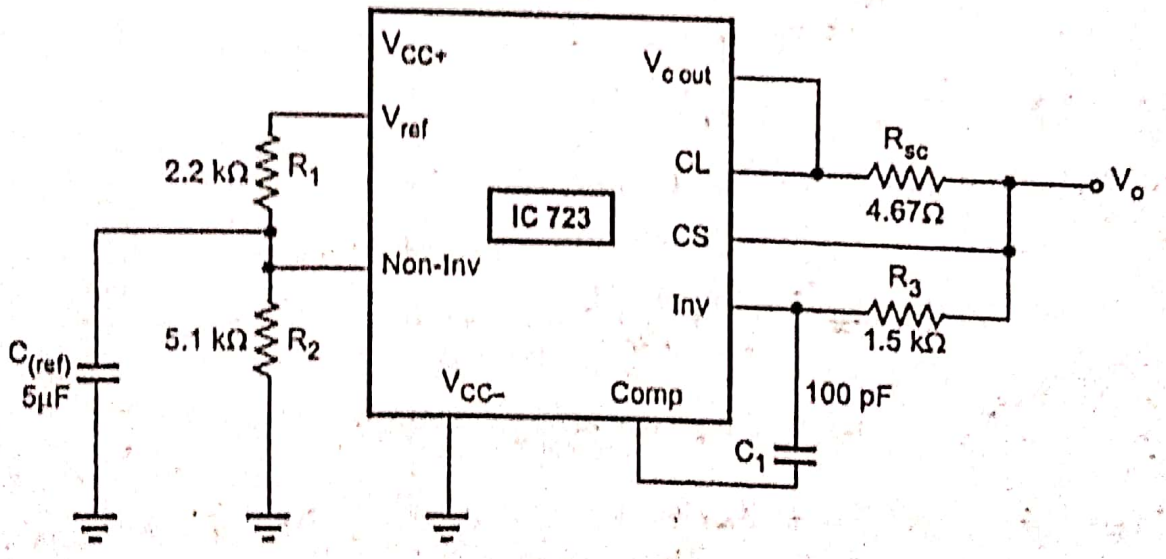


Fig. 7.51

Example 7.11 : *Draw circuit diagram of IC 723 based positive voltage regulator, to give 12 V at 500 mA output. Incorporate short circuit protection limit circuit to operate at 600 mA. Find all resistor values, calculate their wattage and specify the type of resistors.*

Solution : $V_o = 12$ V, $I_L = 500$ mA, $I_{sc} = 600$ mA

It is positive high voltage high current regulator as shown in the Fig. 7.52.

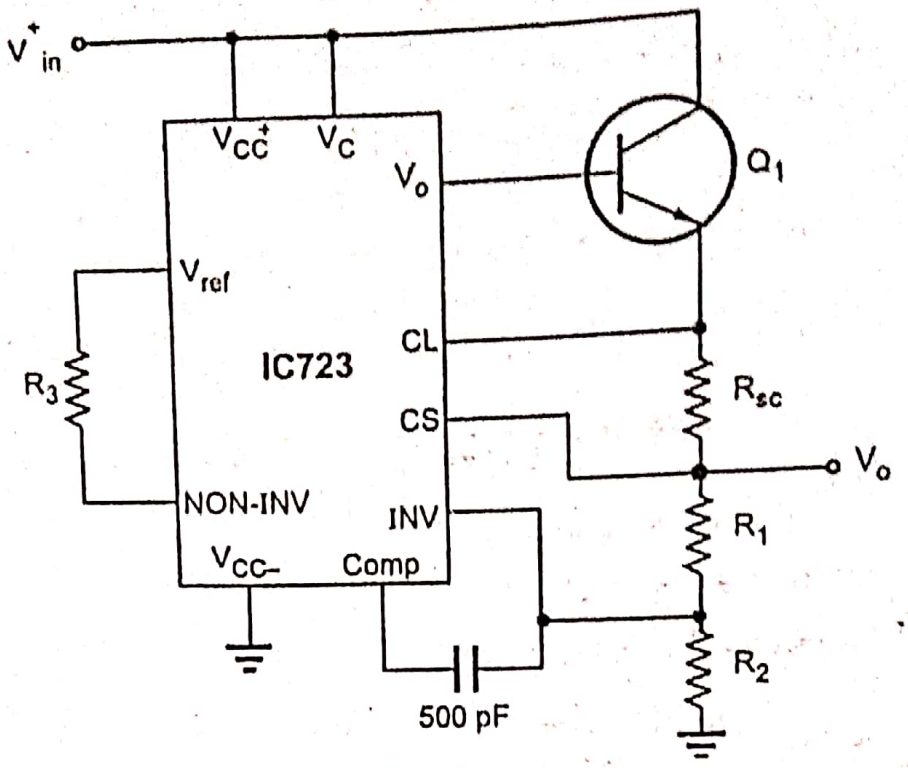


Fig. 7.52

Now $V_o = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right)$

$\therefore \quad 12 = 7\left(\frac{R_1 + R_2}{R_2}\right)$

$\therefore \quad 5\,R_2 = 7\,R_1$

choose $R_1 = 4.7\ k\Omega$

$R_2 = 6.58\ k\Omega \approx 6.8\ k\Omega$ standard value

$R_{sc} = \frac{0.6}{I_{sc}} = \frac{0.6}{600\times100^{-3}} = 1\ \Omega$

$R_3 = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = 2.7\ k\Omega$

Power wattage of $R_{sc} = (I_{sc})^2 R_{sc} = (600\times10^{-3})^2 \times 1 = 0.36\ W = 360\ mW$

All the resistor type can be of metal film resistors. For the power rating of R_1 and R_2 assume the input current to the inverting terminals zero.

$\therefore \quad I = \frac{V_o}{R_1 + R_2} = \frac{12}{(4.7+6.8)\times10^3} = 1.043\ mA$

$\therefore \quad P_1 = I^2R_1 = (1.043\times10^{-3})^2 \times 4.7\times10^3 = 5.112\ mW$

and $P_2 = I^2R_2 = (1.043\times10^{-3})^2 \times 6.8\times10^3 = 7.397\ mW$

So both R_1 and R_2 can be selected safely of 1/16th watt power rating.

: FIELD EFFECT TRANSISTORS:

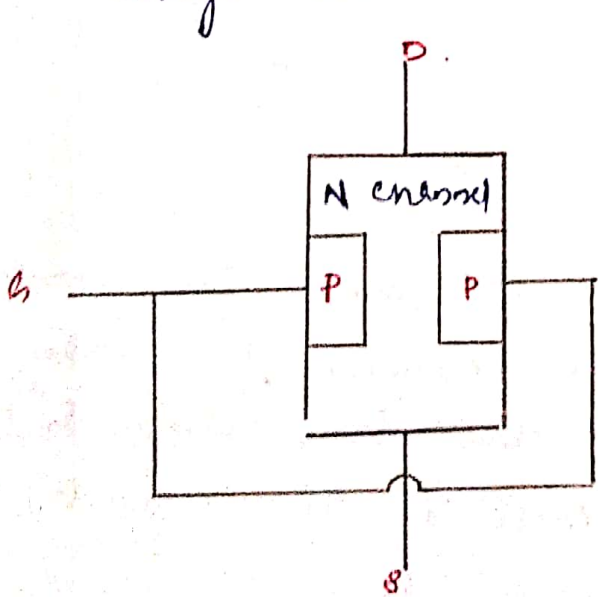
FET is a semiconductor device which depends for its operation on the control of current by an electric field.

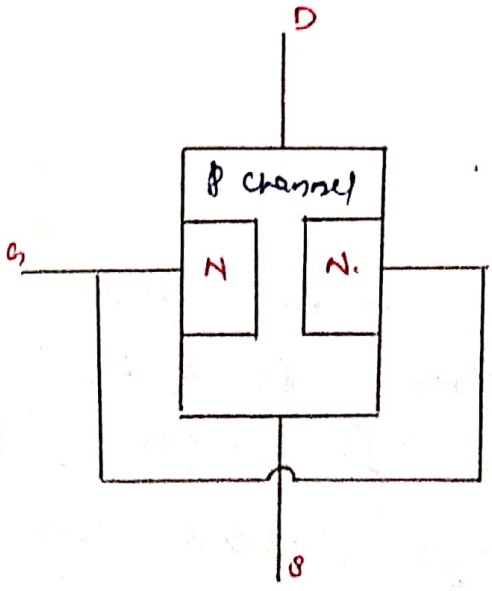
There are two types of FETs: (19)

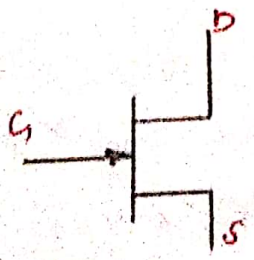
* JFET.
* MOSFETs [Insulated Gate FETs].

: Junction Field Effect Transistors:

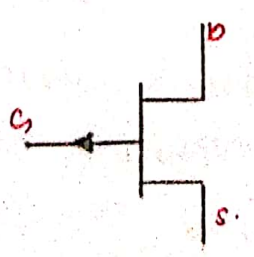
JFET are of two types N-channel and P-channel. In N-channel current conduction the 3 terminals of JFET are Gate, Source and Drain. Gate is controlling terminal. Source is the terminal through which charge carriers enter the device and drain is the terminal through which charge carriers leave the device.







N - channel

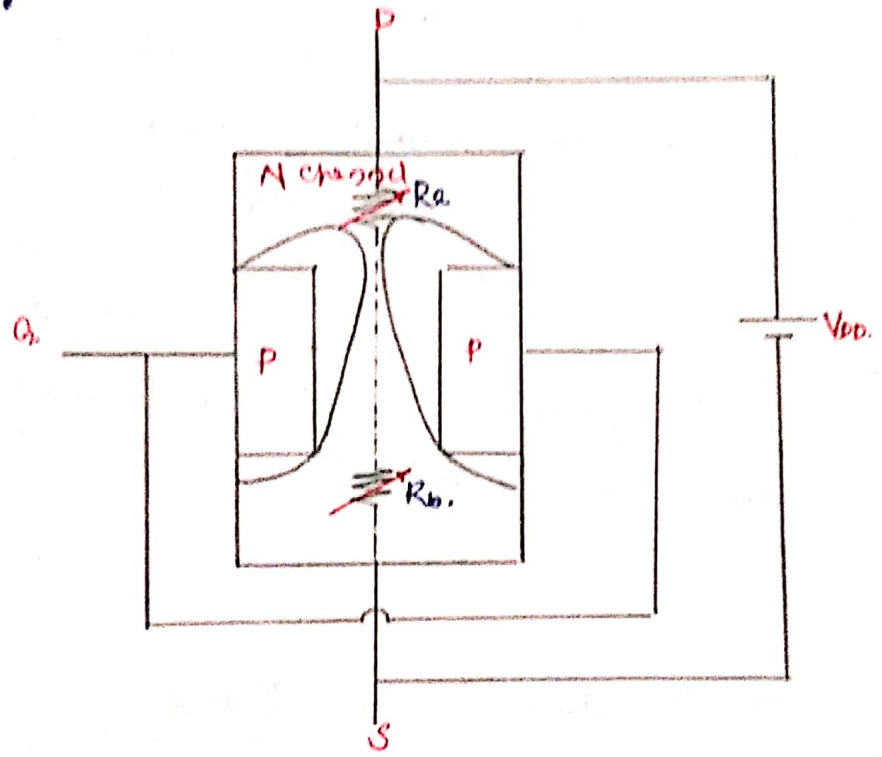


P- channel

Operation of JFET / Depletion layer formation in JFET

Here P type Gate & N type channel constitute a PN junction. This PN junction shown is reverse biased during JFET Operation. In a reverse biased junction there exist depletion region of immobile ions. This depletion region extends in N region where doping concentration is less.

The reverse bias can be obtained by applying voltage across Drain & Source.



In this channel we can assume two channel resistors Ra & Rb. The presence of supply VDD ensures Gate open, ē flow from Source to Drain through channel. and constitute the current known as Drain current ID.

This current causes voltage drop across channel resistance which has the effect of reverse biasing Gate to Source junction. even if Gate is open.

Here depletion region is not symmetrical because of the fact that reverse voltage is higher near the drain end compared to source end of channel.

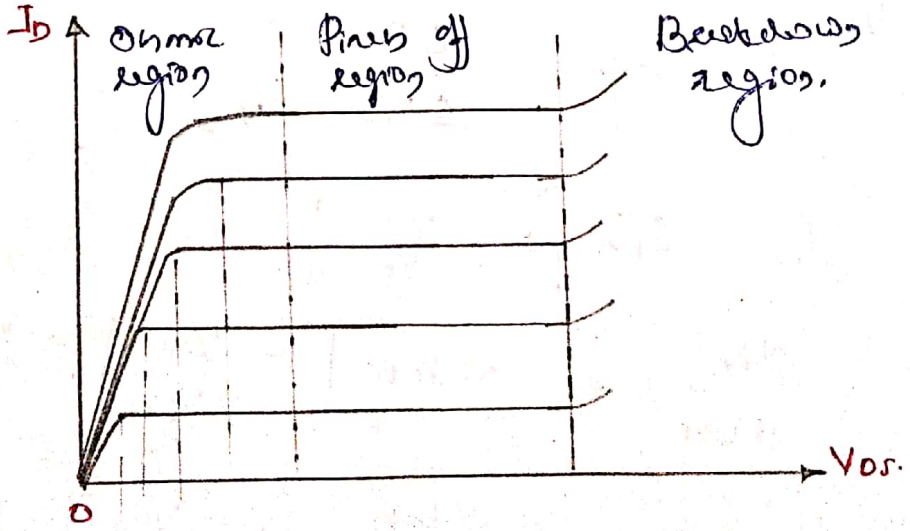
If V_{DS} is increased to a level where it appears that two depletion region would touch each other and is referred as Pinch off. The voltage at which this happens is called pinch off voltage V_p. At pinch off there exists saturation current I_{DSS}.

I_{DSS} is the maximum drain current for JFET and is defined by the condition $V_{GS} = 0$ & $V_{DS} > |V_p|$ The voltage V_{GS} can be used to control the drain current for JFET.

* JFET Characteristics *

VI Characteristics or Drain Characteristics:

It is the graph plotted between Drain current I_D and Drain to Source voltage V_{DS}. for different values of V_{GS}

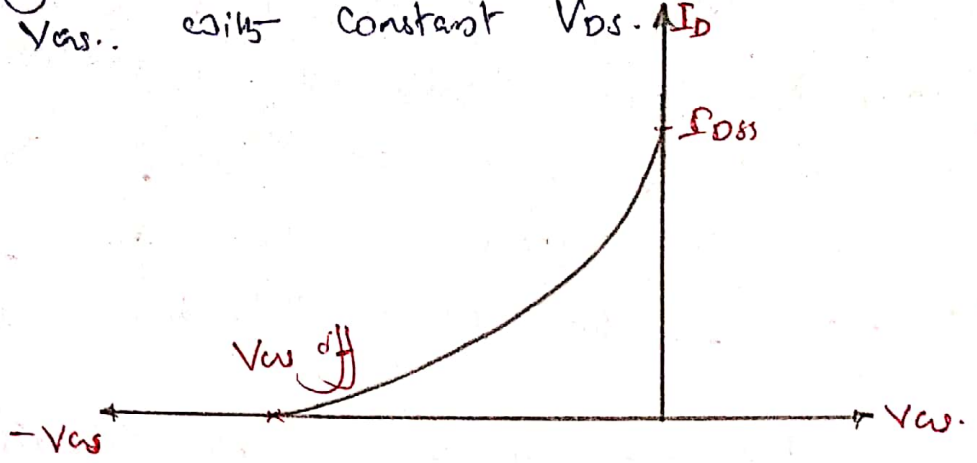


Current relation at Pinch off region

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \Rightarrow \text{Schockley's equation}$$

: Transfer Characteristics:

This is also called Transconductance Curve which gives relationship between Drain Current I_D and V_{GS}. with Constant V_{DS}.



: JFET Parameters:

1.) AC Drain ~~Current~~ resistance (R_d) = Dynamic drain resistance

$$R_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}}$$

2) Transconductance (g_m).

It is the ratio of change in drain current to change in gate to source voltage at constant V_{DS}

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}}$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\frac{dI_D}{dV_{GS}} = 2 I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right] \cdot \frac{-1}{V_P}$$

$$\boxed{g_m = \frac{-2 I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

When $V_{GS} = 0$ $\quad g_{m0} = -2 I_{DSS}/V_P$.

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

3) Amplification factor (μ)

It is the ratio of change in V_{DS} to change in V_{GS} at constant drain current.

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = R_d \cdot g_m}$$

4) DC drain resistance R_D.

It is also called static or Ohmic resistance.

$$R_D = \frac{V_{DS}}{I_D}$$

(19)

Comparison between JFET & BJT.

JFET	BJT.
1. Unipolar device conduction occurs due to flow of either e^- or hole.	* Bipolar device conduction occurs due to both e^- & hole
2. Voltage controlled device Gate voltage controls drain current	* Current controlled device Base current controls collector current
3. High i/p impedance (MΩ)	* low i/p impedance (kΩ)
4. Negative temp coefficient	* Positive temp coefficient
5. Higher Switching Speed	* Lower Switching Speed
6. Generate less noise	* Generate more noise
7. Occupies less space in IC	* Occupies more space in IC
8. power consumption is low	* High power consumption.

Metal Oxide Semiconductor FET. (MOSFET)

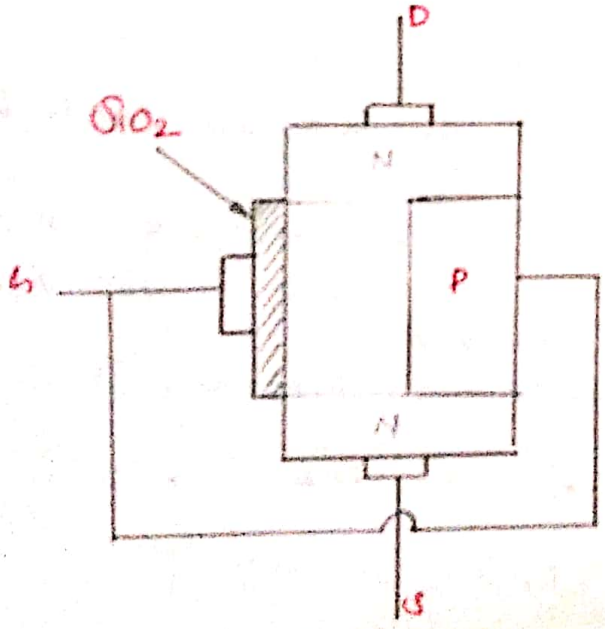
MOSFET is also called as Insulated Gate FET (IGFET). There is no direct electrical contact between gate & channel of MOSFET. Due to the presence of Insulator (SiO_2) between gate & channel MOSFET poses very high i/p impedance. and there is no gate current.

MOSFETs are of two types depending on whether the channel is already present or not,

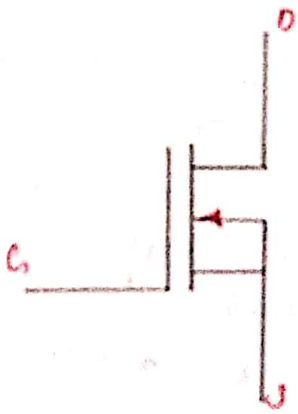
* Depletion type MOSFET
* Enhancement type MOSFET.

D-MOSFET

D type MOSFET is the one in which there exists an inherent channel.



N channel D MOSFET



Symbol.

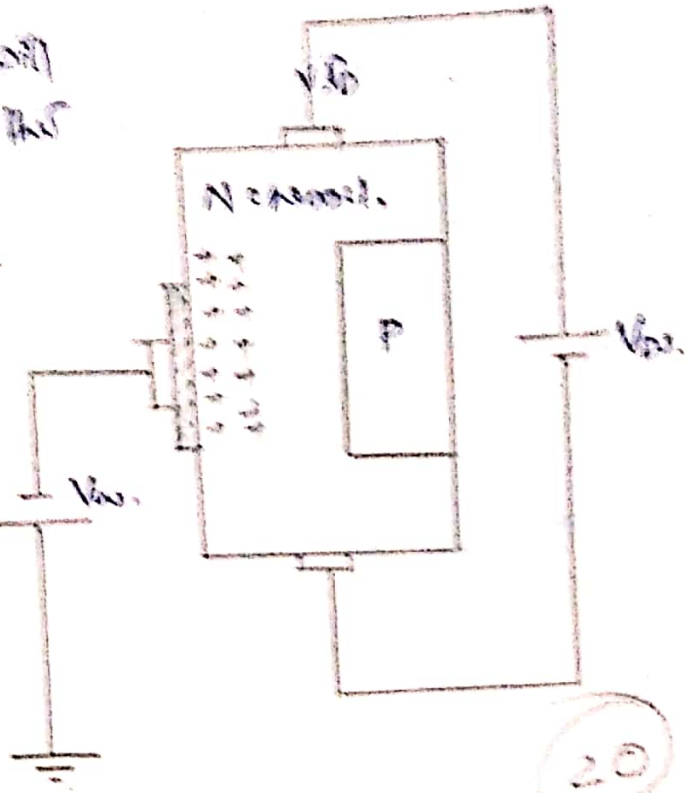
Operation

when $V_{GS}=0$ and V_{DS} is applied then Drain & Source. This results in attraction of $\bar{e}$ in channel towards the potential of Drain terminal and drain

current is controlled through N channel.
This current Id with Vds is called Idss
as in JFET.

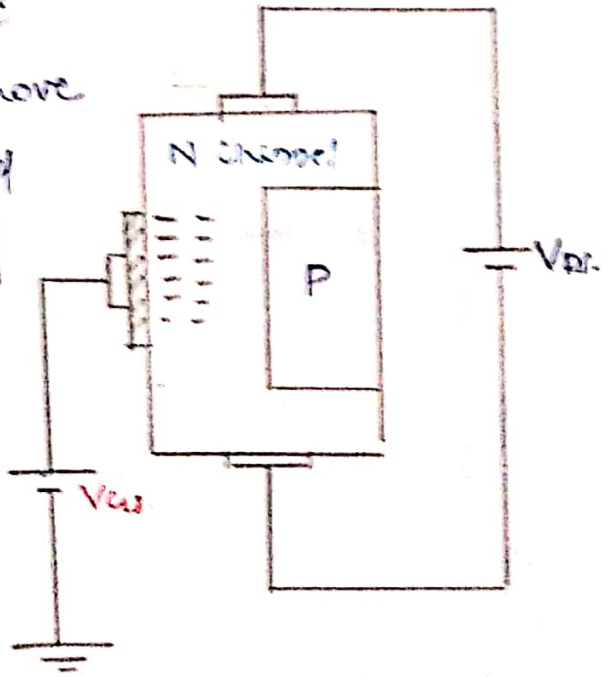
Depletion mode of Operation:

when V_{GS} is -ve, it will attract the holes towards the gate end of channel.
This tends to reduce the effective width of channel and this reduces the conductivity and therefore Drain current decreases.

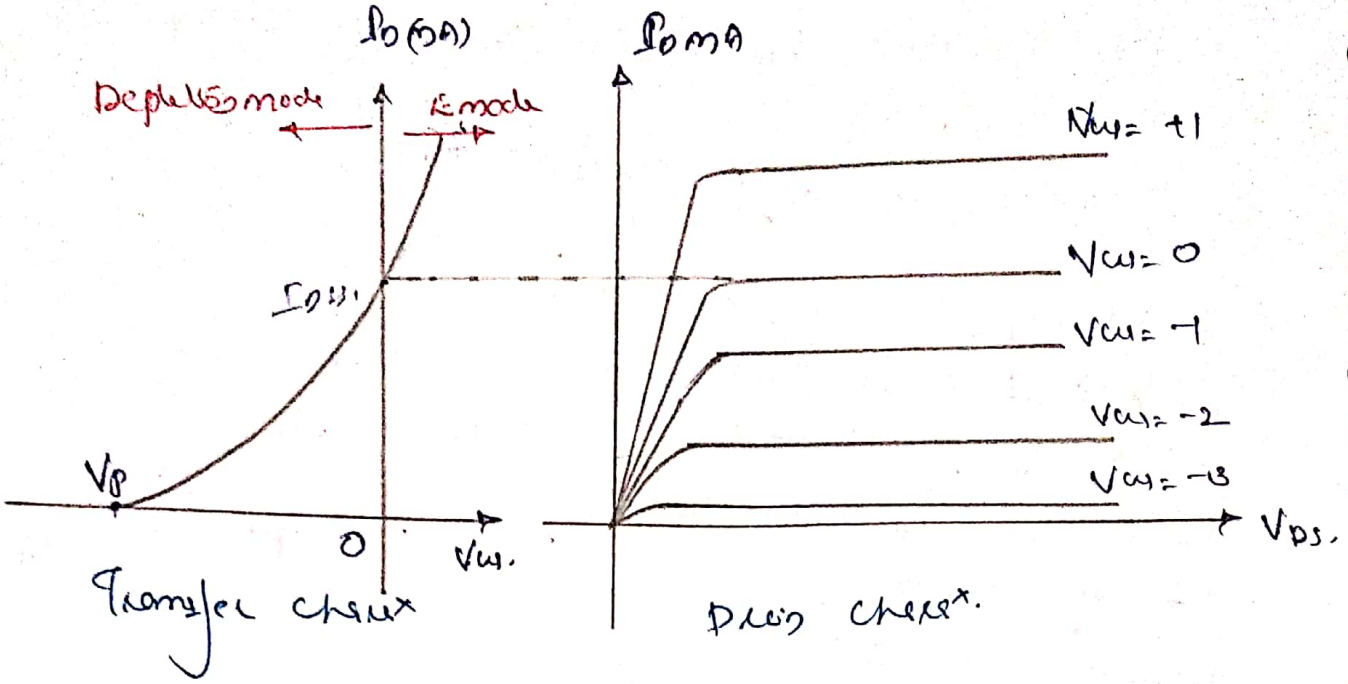


Enhancement mode of Operation:

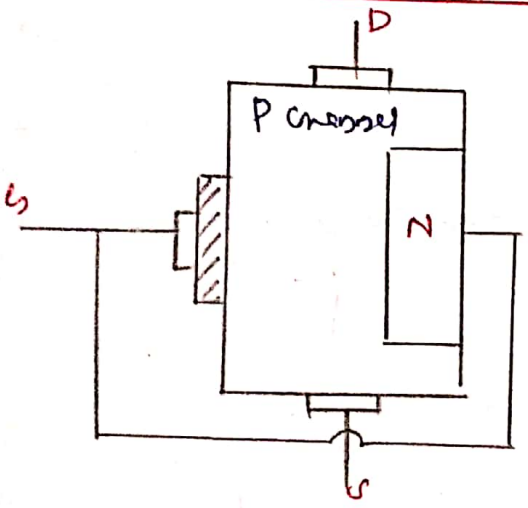
The positive gate voltage causes free electrons to move from substrate to channel and resulting in increased drain current.
This drain current increases with increase in V_{GS}. Hence channel is enhanced during the V_{GS}.



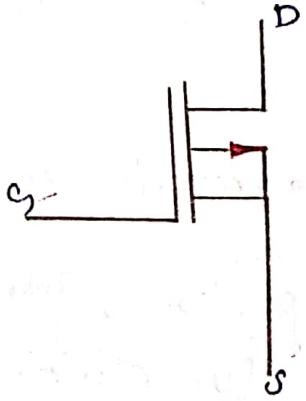
Current equation Id: R[



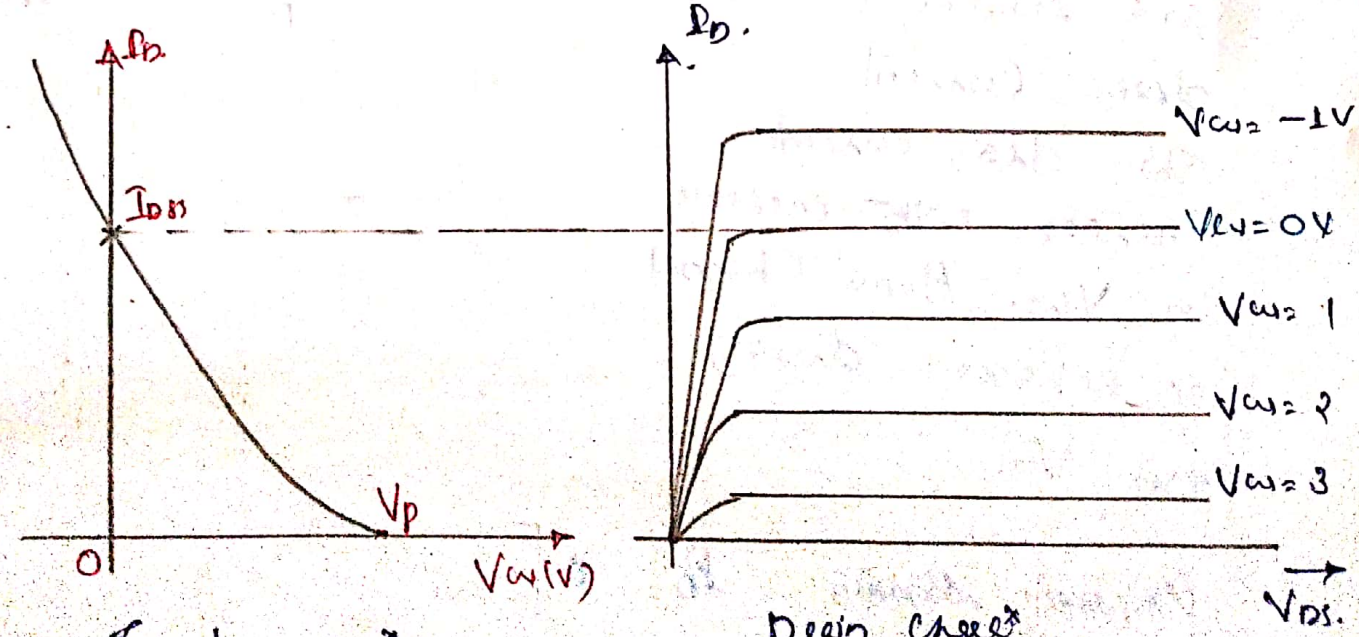
P- Channel D- MOSFET.



Structure

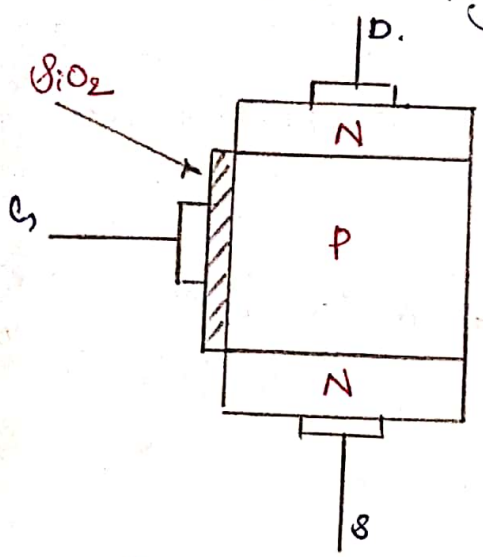


Symbol.

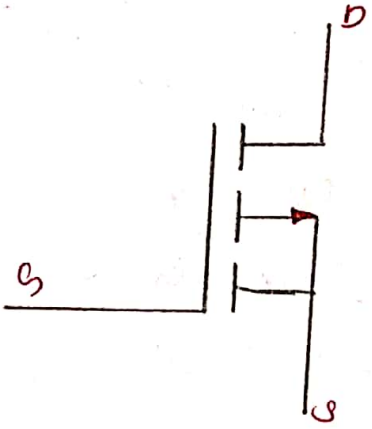


Enhancement Type MOSFET.

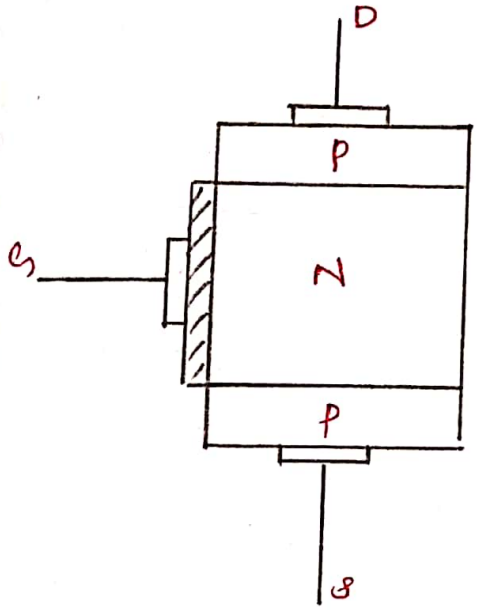
In E-MOSFET, there is no inherent channel. It can work only in Enhancement mode.



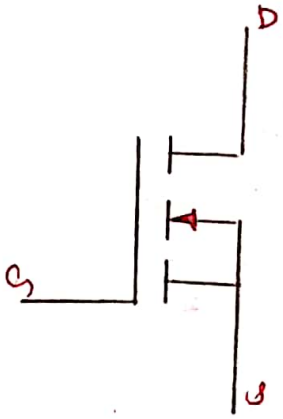
P Channel MOSFET



Symbol.



N Channel MOSFET

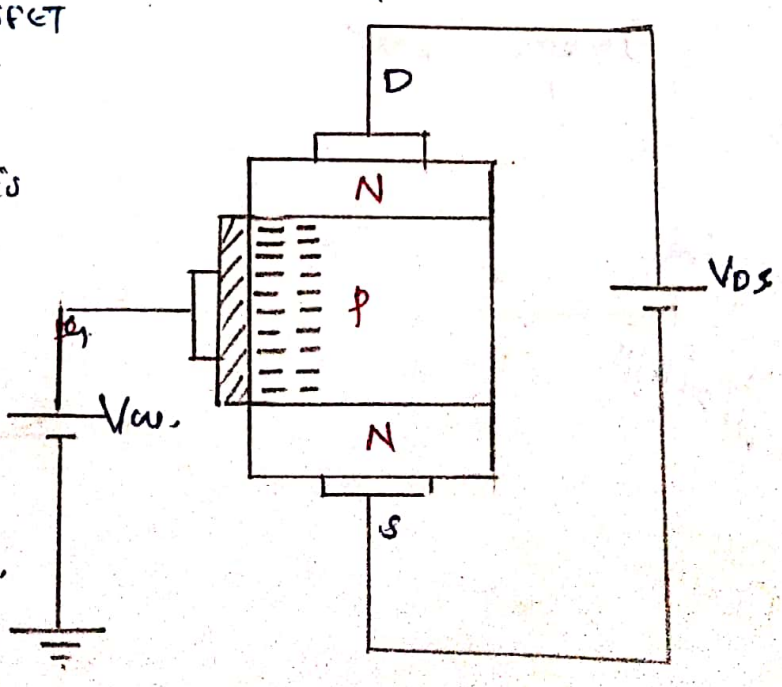


Symbol.

21

Operation

In E MOSFET there is no inherent Channel. By the application of +ve V_{GS}, it will attract e to the gate end of MOSFET.

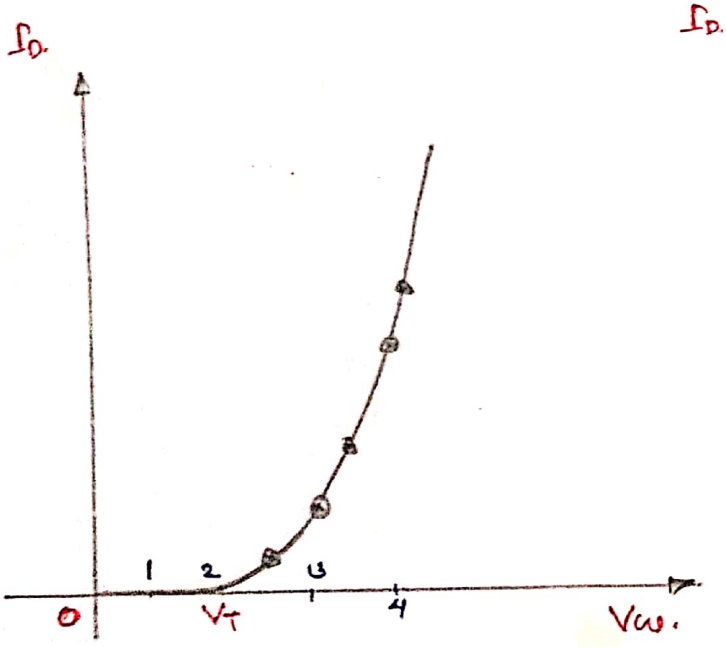


and thus by creates a layer of $\bar{e}$ which creates a channel b/w Drain & Source. ∴ Drain Current I_D flows through the device

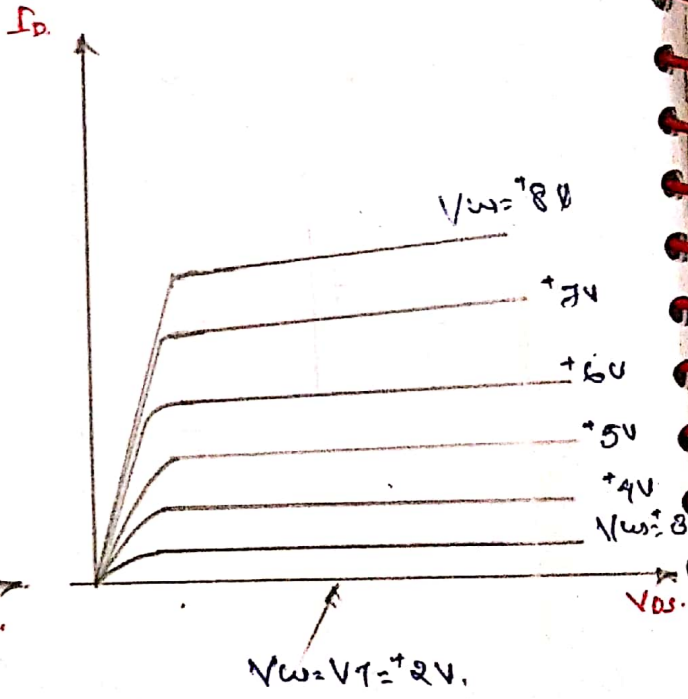
$$I_D = K[V_{GS} - V_{GS_{TH}}]^2$$

$V_{GS_{TH}}$ is the voltage at which channel is created b/w Drain & Source

The gate to Source voltage required to create a channel between Source & Drain and thus to turn ON the transistor is known as Threshold Voltage



Transfer Char^x



Drain Charax.

Verified
22/8/16
18/11/16

MODULE 3

MODULE III

AMPLIFIERS:

Biasing of Transistor:

The basic function of transistor is amplification. The process of raising the signal strength of a weak signal without any change in its general shape is known as faithfull amplification. For faithfull amplification it is necessary that

1. Base Emitter - Base junction forward biased
2. CB junction Reverse biased
3. proper Zero Signal collector current.

The proper flow of Zero signal collector current I_C and maintenance of proper V_{CE} during change of signal is called Transistor biasing

Bias Stabilization:

Only fixing of Operating point is not sufficient, it must also ensure that it should remain there where it was fixed.

There are two reasons for operating point to shift.

* Transistor parameters are temperature dependent
* The parameter β varies from unit to unit.

The maintenance of Operating point stable (independent of temperature variations and variations in transistor parameters is known as Bias Stabilization.

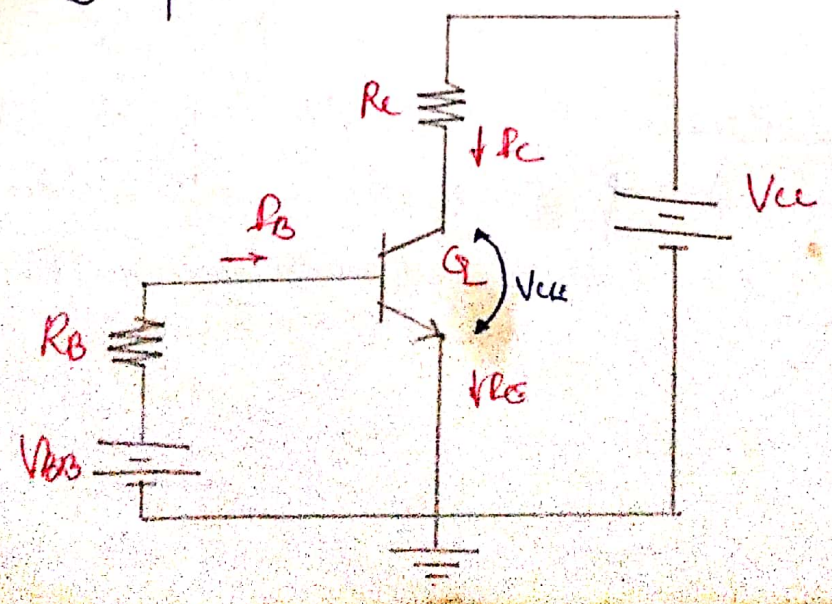
Flow of current in collector circuit produce heat at collector ckt. This increases the temperature and more minority carriers are generated in base collector junction. Since more bonds are broken and resulting leakage current I_{CO} (I_{CBO}) increases.

$$I_C = \beta I_B + (\beta+1) I_{CBO}.$$

Increase in I_{CBO} increases I_{CEO} and this in turn increase collector current I_C. Cumulative increase in I_C will ultimately shift operating point. Thus even heat produces at junction and not even burn the transistor. Such situation is called thermal run away.

Operating point & DC load line.

For proper operation of transistor, whether the signal (ac input) is present or not, a fixed level of current and voltages are required. These voltage & current define a point at which the transistor operates. This point is called Operating point or Quiescent point.



Applying KVL to o/p ckt

$$V_{cc} - I_c R_c - V_{ce} = 0.$$

$$I_c = \frac{-1}{R_c} V_{ce} + \frac{V_{cc}}{R_c} \quad \text{--- (1)}$$

eqn (1) can be equated to eqn for a line

i.e $y = mx + c$

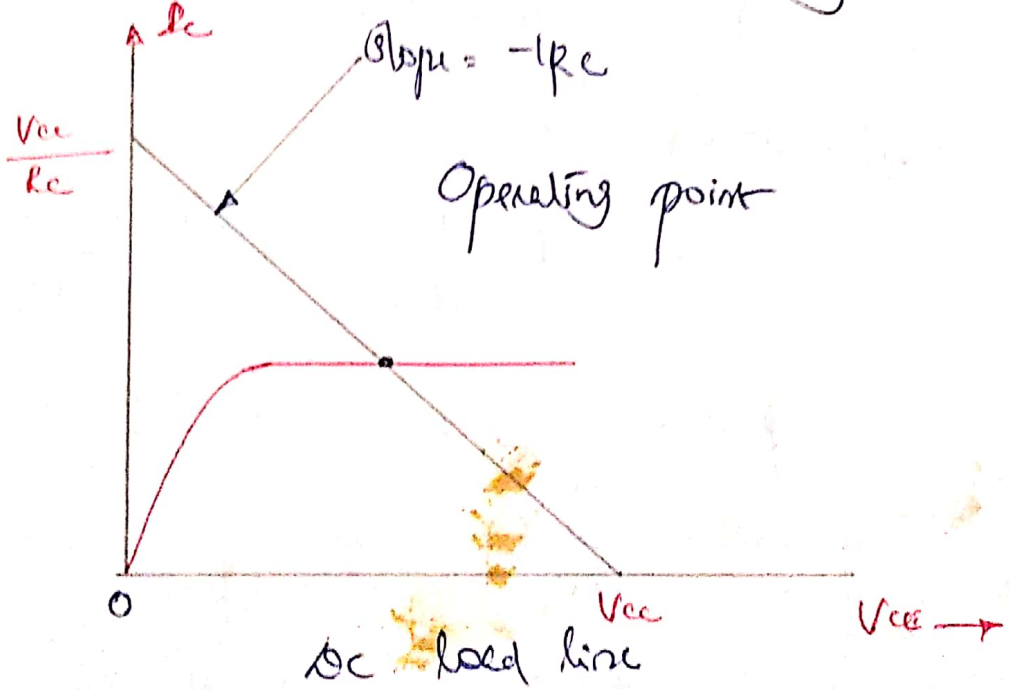
$y = I_c$; $m = -1/R_c$ $x = V_{ce}$ $c = \frac{V_{cc}}{R_c}$

i eqn (1) defines a line

when $I_c = 0$; $V_{ce} = V_{cc}$

$V_{ce} = 0$ $I_c = V_{cc}/R_c$

These two values are two ends of load line.



DC load line

DC load line can be defined as a line on o/p characteristics of transistor which gives values of I_c and V_{ce} corresponding to zero signal conditions.

DC load line gives following information

* load line intersects the horizontal base axis at a point marked V_{cc} which is called

transistor cutoff point. At this point $I_B = I_C = 0$.

* The load line intersects vertical axis at point marked $\frac{V_{cc}}{R_c}$ is called saturation point. At this point I_C is maximum & $V_{CE} = 0$.

Stability factor:

Stability factor 'S' is defined as the rate of change of collector current w.r.t I_{co} keeping β & V_{BE} constant.

$I_{co} = I_{CBO}$

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

$$I_C = \beta I_B + (\beta+1) I_{co} \quad \ldots (1)$$

Differentiating eqn (1) w.r.t I_C

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{\partial I_{co}}{\partial I_C}$$

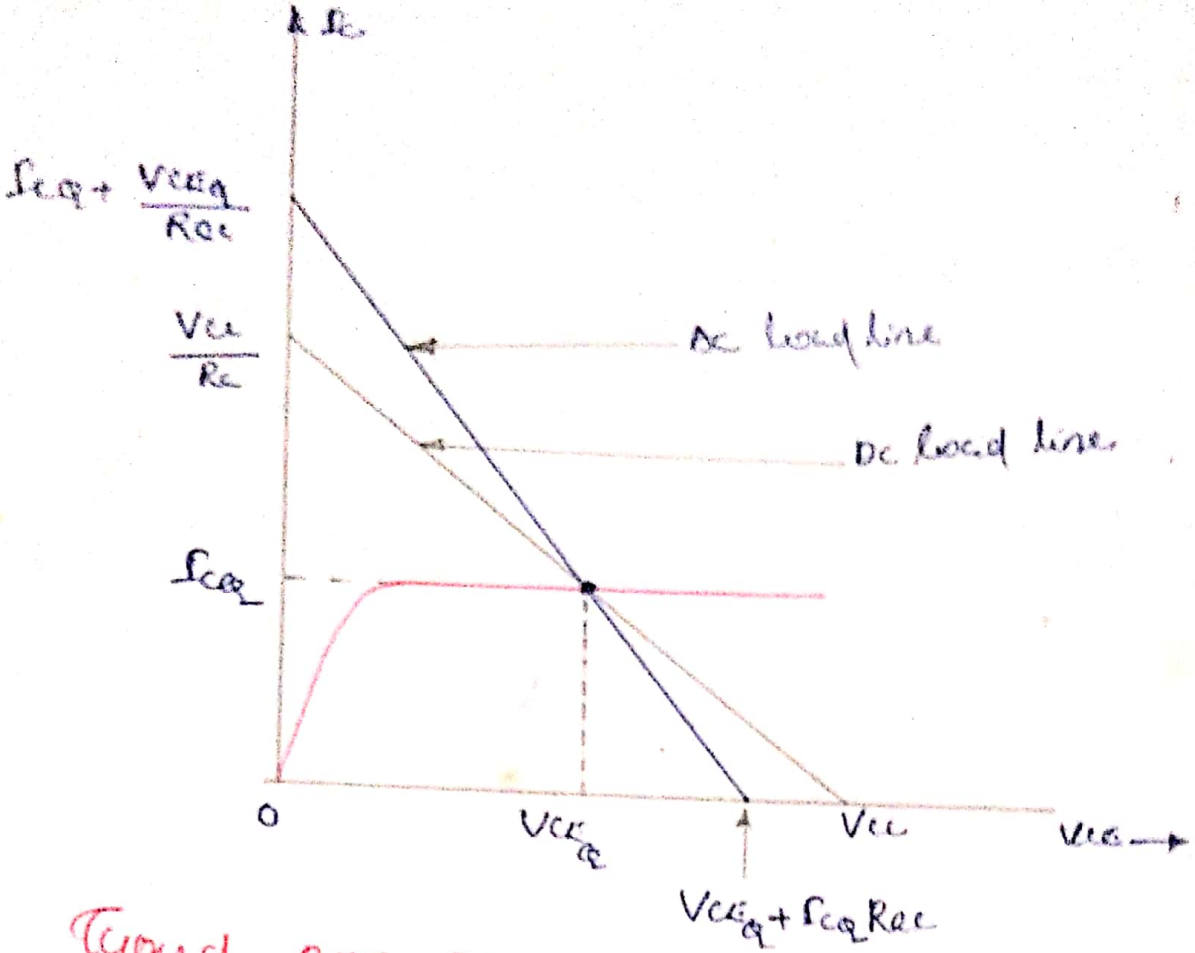
$$(\beta+1) \frac{\partial I_{co}}{\partial I_C} = 1 - \beta \frac{\partial I_B}{\partial I_C}$$

$$S = \frac{\partial I_C}{\partial I_{co}} = \frac{(\beta+1)}{1 - \beta \frac{\partial I_B}{\partial I_{co}}}$$

Ac load line:

The ac load line gives the values of V_{CE} and I_C when ac signal is applied. Ac load line takes into account the ac load resistance while dc load line considers the only dc load resistance.

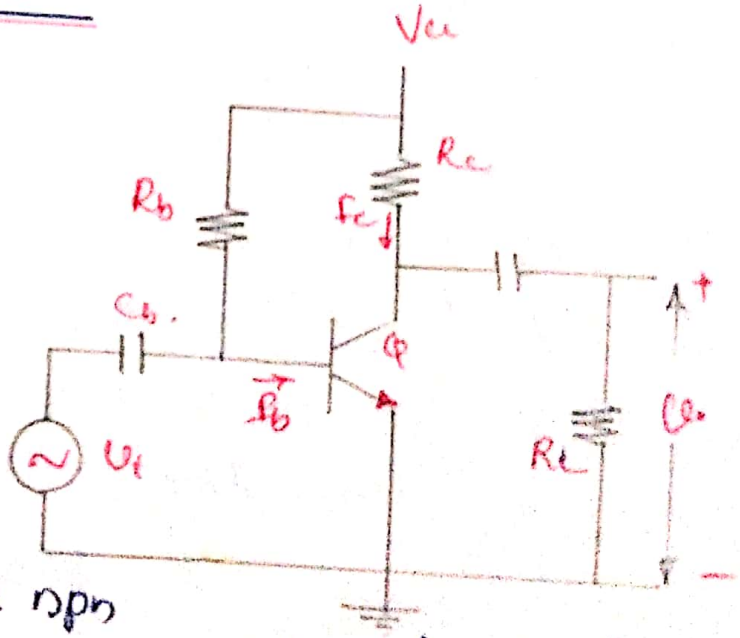
ac load resistance $R_{ac} = R_c \| R_L$



Types of BJT Biasing:

Fixed Biasing:

It is also known as Base bias ckt. Here the resistance R_b provides fixed bias voltage to the base



The ckt consists of npn transistor, R_c and base resistance R_b, load R_L.

Resistance R_b is selected to obtain required I_b.

Applying KVL to i/p side; $V_{cc} - I_b R_b - V_{BE} = 0$.

$$R_b = \frac{V_{cc} - V_{BE}}{I_b} \quad ; \quad \because V_{cc} > V_{BE}$$

$$\simeq \frac{V_{cc}}{I_b} //$$

This means I_B is constant & fixed

Stability factor for fixed bias ckt

We have $I_C = \beta I_B + (\beta+1) I_{CO}$.

Diff w.r.to I_C

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{\partial I_{CO}}{\partial I_C}$$

But I_B is independent of I_C. $\therefore \frac{\partial I_B}{\partial I_C} = 0.$

$$\frac{\partial I_C}{\partial I_{CO}} = \beta + 1$$

$$\boxed{S = \beta + 1}$$

* With fixed bias ckt, it is easy to fix Quiescent Operating point anywhere in active region of the chart by simply changing the value of resistor R_B. It provides maximum flexibility in design.

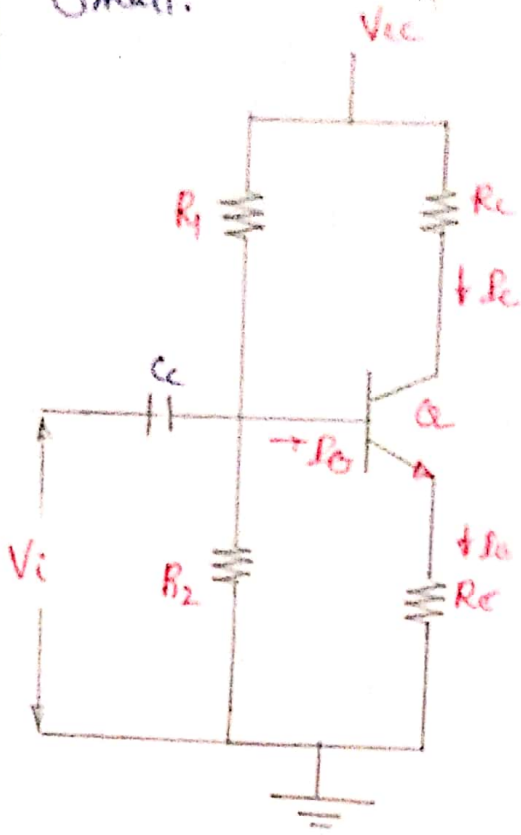
Why fixed Bias ckt is seldom used

* But with β is temperature collector Current I_C goes on increasing & thus by increasing temp again & cause thermal Runaway.

* We know $I_C = \beta I_B$; Here I_B is fixed, $\therefore$ Current I_C is solely depend on β. when transistor is replaced by another one with different value of β, operating point will shift. The stabilization of operating point is very poor.

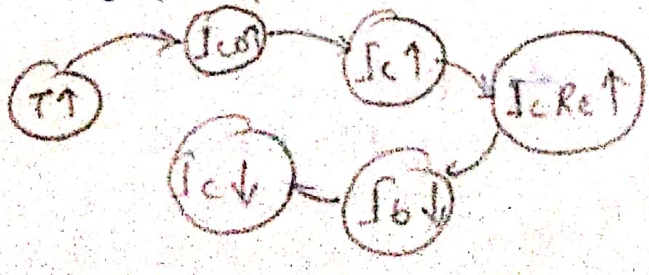
Self Bias or Voltage Divider Bias ckt:

This ckt is used when collector resistance R_c is very small.



The current in emitter R_e causes voltage drop in a direction to reverse bias the emitter base junction. For transistor to remain in active region E-B junction has to be forward biased, the required bias is obtained from power supply through potential divider N/w R_1 & R_2.

If I_c tends to increase due to increase in I_{co} with temperature, voltage drop across R_e increases there by decreasing base current I_b. So I_b & I_c maintained at almost const.

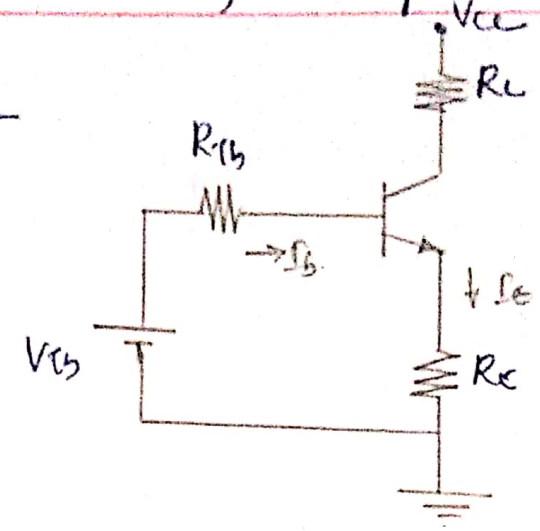


Thevenin Equivalent ckt of Voltage divider bias ckt

Here $V_{TH} = V_{cc} \times \frac{R_2}{R_1+R_2}$

$R_{TH} = R_1 \| R_2$

$= \frac{R_1 R_2}{R_1+R_2}$



Stability factor (S)

$$S = \frac{\partial I_c}{\partial I_{co}} = \frac{\beta+1}{1-\beta \frac{\partial I_B}{\partial I_c}} \quad \text{--- (1)}$$

Applying KVL in i/p side of equivalent ckt

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0.$$

$$V_{TH} - I_B R_{TH} - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{TH} - I_B (R_{TH} + R_E) - V_{BE} - I_C R_E = 0.$$

$$I_B = \frac{V_{TH} - V_{BE} - I_C R_E}{R_{TH} + R_E}.$$

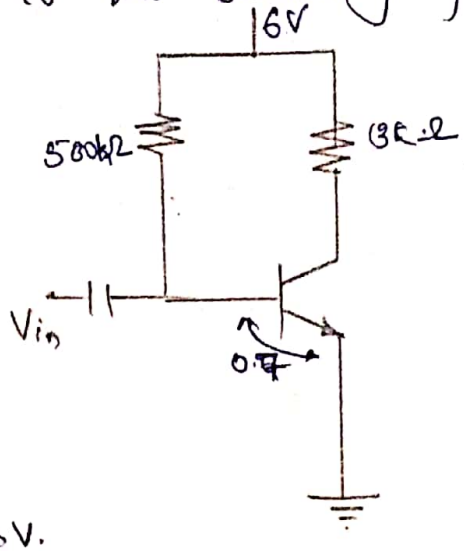
$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_{TH}+R_E} \quad \text{--- (2)}$$

Sub: eqn (2) in (1)

$$S = \frac{\beta+1}{+1+\beta \frac{R_E}{R_E + R_{TH}}}$$

Problem.

(1) In a fixed bias compensation ckt, a Silicon transistor with $\beta = 100$ is used, $V_{cc} = 6V$, $R_c = 3K\Omega$, $R_B = 530K\Omega$. Draw the load line & determine the Operating point. what is the stability factor.



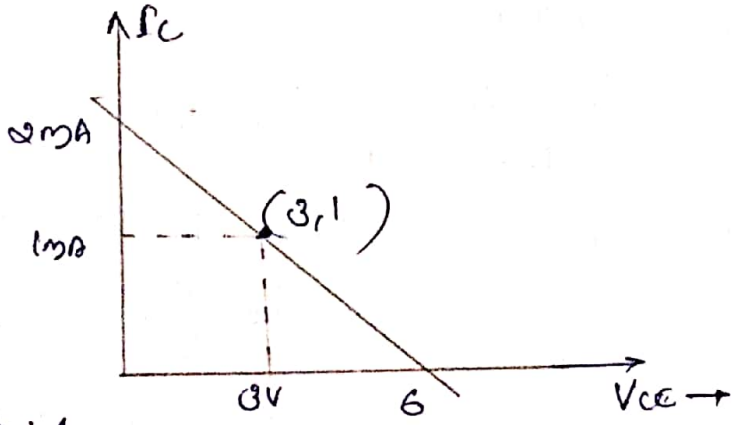
DC load line

KVL at o/p.

$V_{cc} - I_c R_c - V_{CE} = 0$.

$I_c = 0$; $V_{CE} = V_{cc} = 6V$.

$V_{CE} = 0$; $I_c = \frac{V_{cc}}{R_c} = \frac{6}{3k} = 2mA$



Operating point

KVL in input side

$V_{cc} - I_B \times 530k - 0.7 = 0$

$I_B = \frac{5.3}{530k} = 10\mu A$.

$I_c = \beta I_B = 100 \times 10\mu = 1mA$.

KVL in o/p side $6 - 1mA \times 3k - V_{CE} = 0$.

$V_{CE} = 3V$

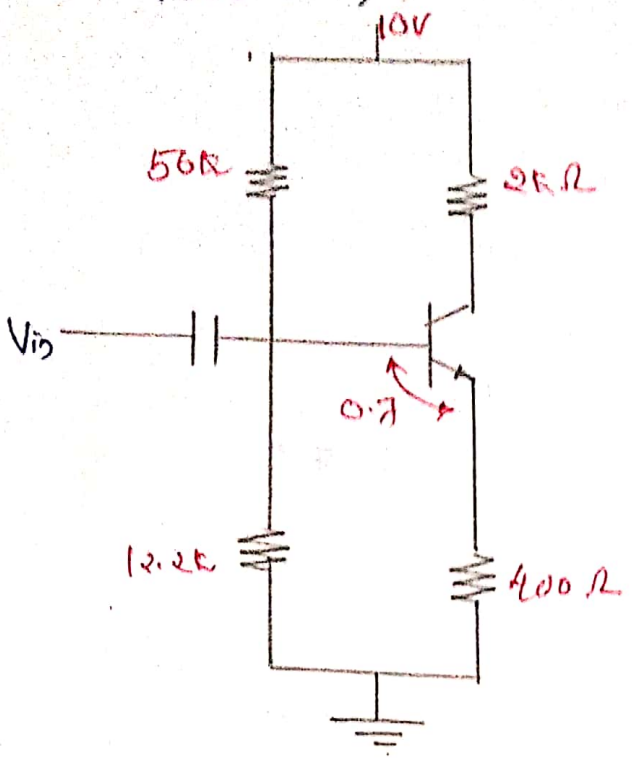
$Q = (3V, 1mA)$

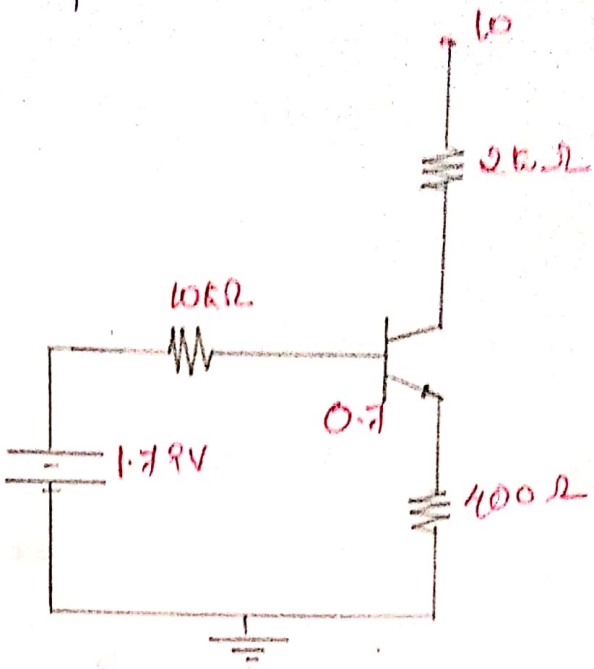
stability factor $S = \beta + 1 = 101$

Q) Given the voltage divider bias ckt, determine Q point

Ans $R_1 = 56K\Omega$, $R_2 = 12.2K\Omega$, $R_C = 2K\Omega$, $R_E = 400\Omega$,

$V_{CC} = 10V$, ; $V_{BE(on)} = 0.7V$, $\beta = 150$





$R_{Th} = 56K \parallel 12.2K = 10K\Omega$

$V_{Th} = 10 \times \frac{12.2K}{12.2K + 56K} = 1.79V$

KVL in i/p side $1.79V - I_{BQ}10K - 0.7 - (\beta+1)I_B \times 400 = 0$

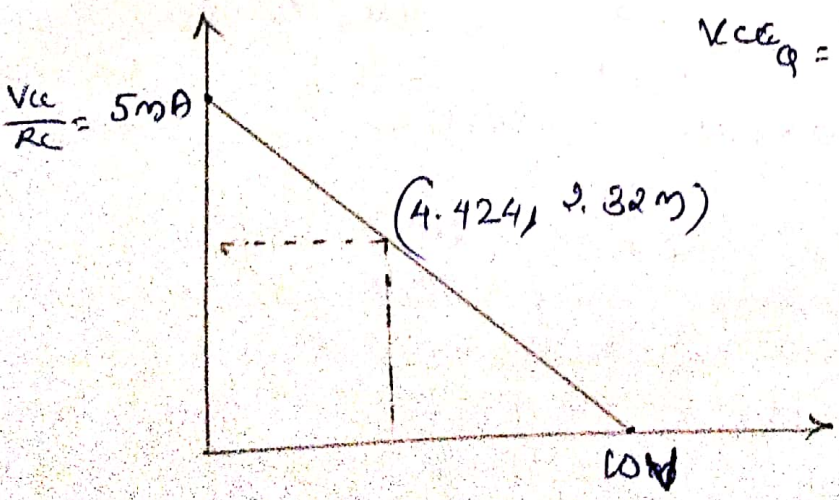
$I_{BQ}[10K + 151 \times 400] = 1.09$

$I_{BQ} = \underline{15.48\,\mu A}$ $I_{CQ} = \underline{2.34\,mA}$

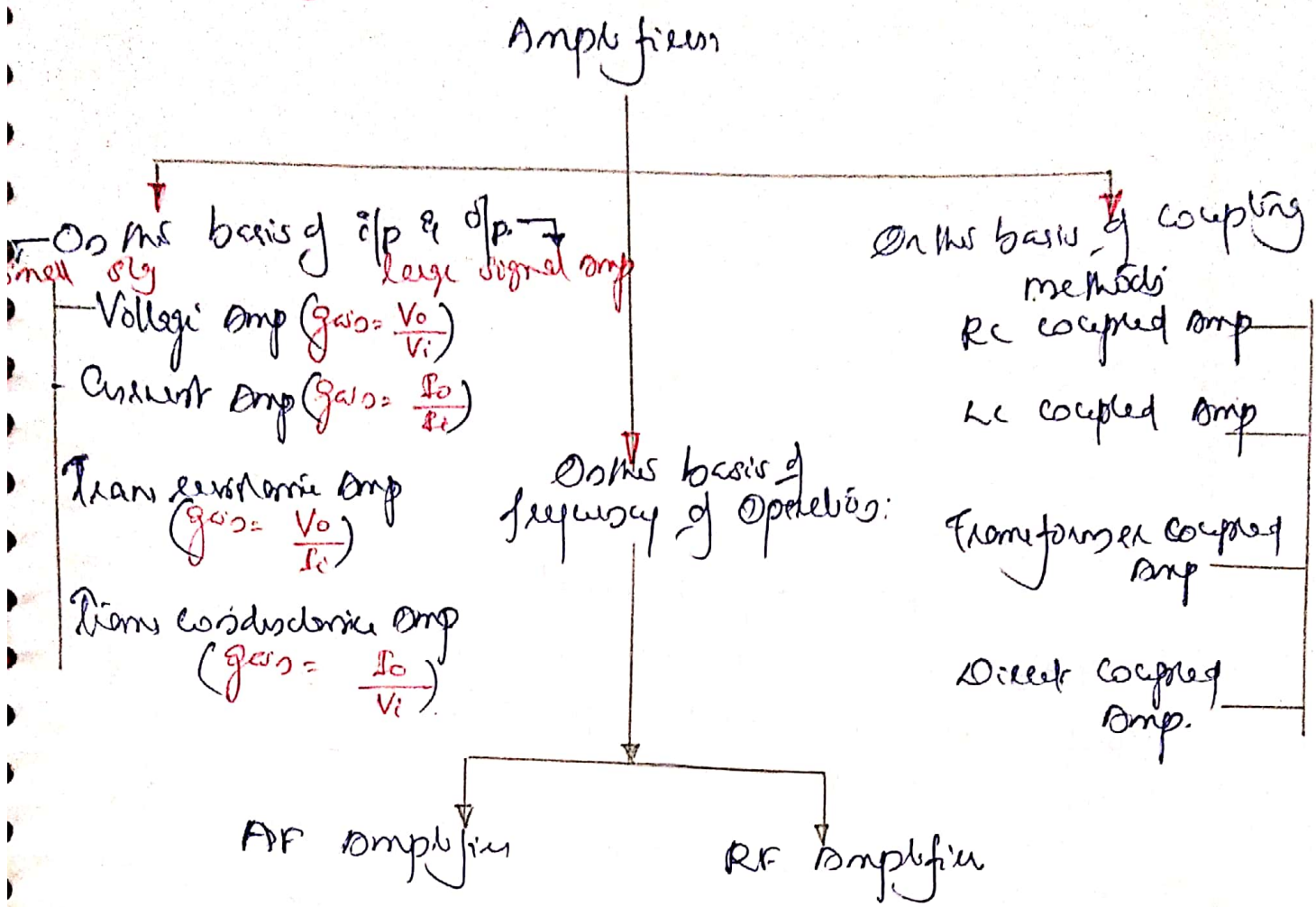
$\therefore I_{CQ} = 15.48 \times 150 = \underline{2.32mA}$

KVL in o/p $10 - 2K \times 2.32m - V_{CE} - 2.34m \times 400 = 0$

$V_{CE_Q} = 4.424$



Classification of Amplifiers:

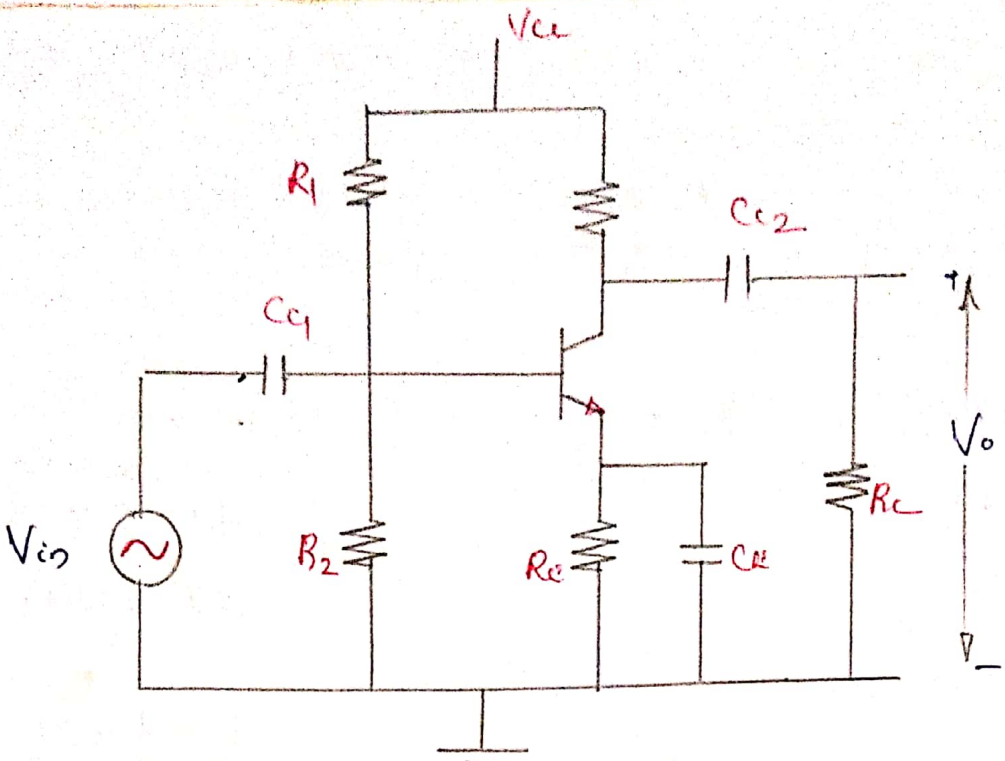


: RC Coupled Amplifier :

It is a CE amplifier used in audio frequency applications. For proper functioning of amp^r transistor must be in active region. where base current has complete control over collector current

$I_c = \beta I_B$.

It is a voltage amplifier and its coupling b/w successive stages are done by Resistance - Capacitance coupling. Voltage divider biasing is used in this ckt



RE coupled Amp^{r}.

R_1 & R_2 are called potential dividers which is fixed across Vcc and ground. It provides better stability for the ckt

C_{c1} & C_{c2} are coupling capacitors. which blocks dc component from one stage to other. C_{c1} couples Vin to input of amplifier. C_{c2} used to block dc component of o/p voltage from entering load resistor Rc.

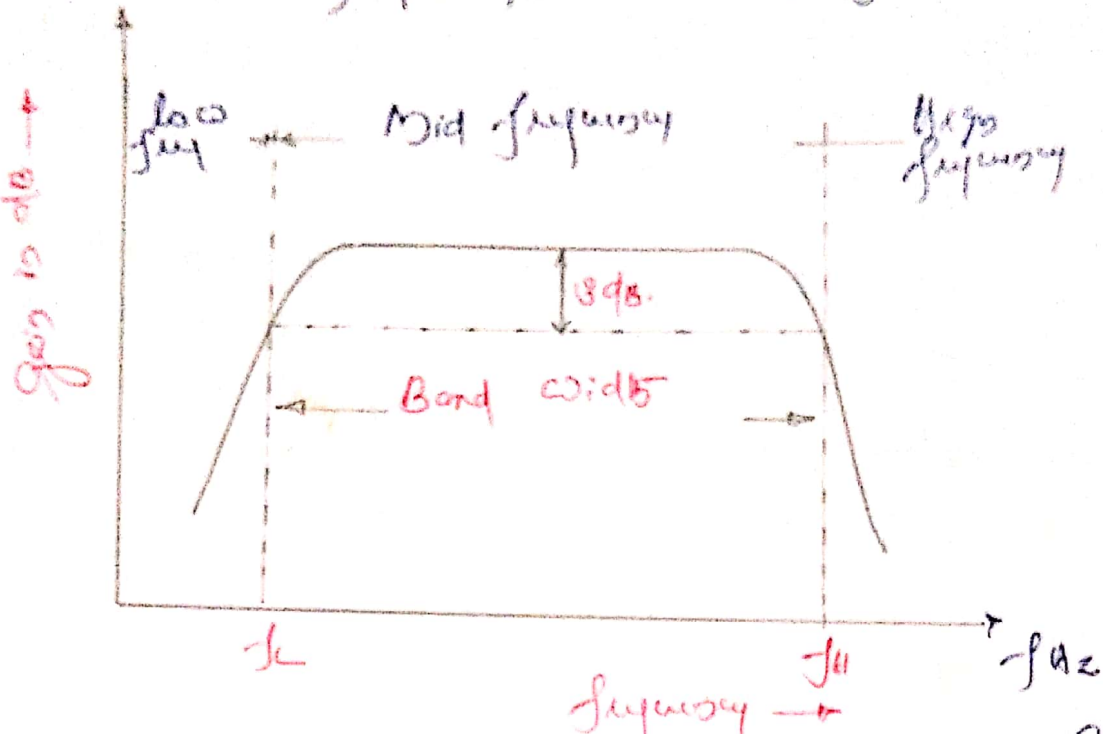
RE stabilizes operating point against temperature variations.

CE is the bypass capacitor which bypass ac signal developed across RE to ground. The reactance of CE should be much less than RE

$$X_{CE} \leq \frac{R_E}{10}.$$

Frequency Response of RC coupled Amplifier

Frequency response of an amplifier can be graph plotting between frequency (x-axis) & gain (y-axis).



In the frequency response plot we can see gain roll-off at low and high frequency ranges. and constant gain at mid frequencies.

At low frequencies

At low frequencies the reactances of coupling capacitors C_{c1} & C_{c2} will be very high $\left[X_C = \frac{1}{2\pi fC}\right]$ and therefore i/p signal voltage will not couple properly to amplifier and the amplified o/p will not couple properly to load ∴ gain reduces at low frequencies

At high frequencies

At high frequencies inter electrode capacitances and stray wiring capacitance plays a major role in reducing the gain. At high frequencies these capacitance will act

as short ckt ∴ o/p signal will be shorted to ground before it reaches amplifier and the o/p of amplifier also shorted to ground before it reaches to load ∴ gain will be reduced at high frequencies.

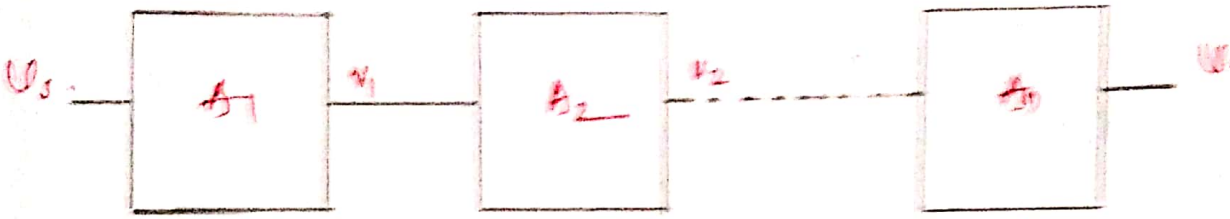
At mid frequencies there less effects compensate each other to give constant gain.

Here the Bandwidth of an amplifier is defined as the range of frequencies over which the amplifier provides desired gain.

$$BW = f_H - f_L$$

: Multistage Amplifiers :

When amplification of a single stage amplifier is not adequate, the gain can be increased by connecting two or more stages of amplification. Such configuration is called multistage amplifier.



BD of multistage amplifier

Here o/p of 1st stage makes the input of 2nd stage, o/p of 2nd stage makes input of 3rd stage and so on..... the signal V_s is applied to the input of 1st stage

o/p of 1st stage $V_1 = A_1 V_s$

o/p of 2nd stage $V_2 = A_2 V_1$

final o/p $V_o = V_n = A_n \cdot V_{n-1}$

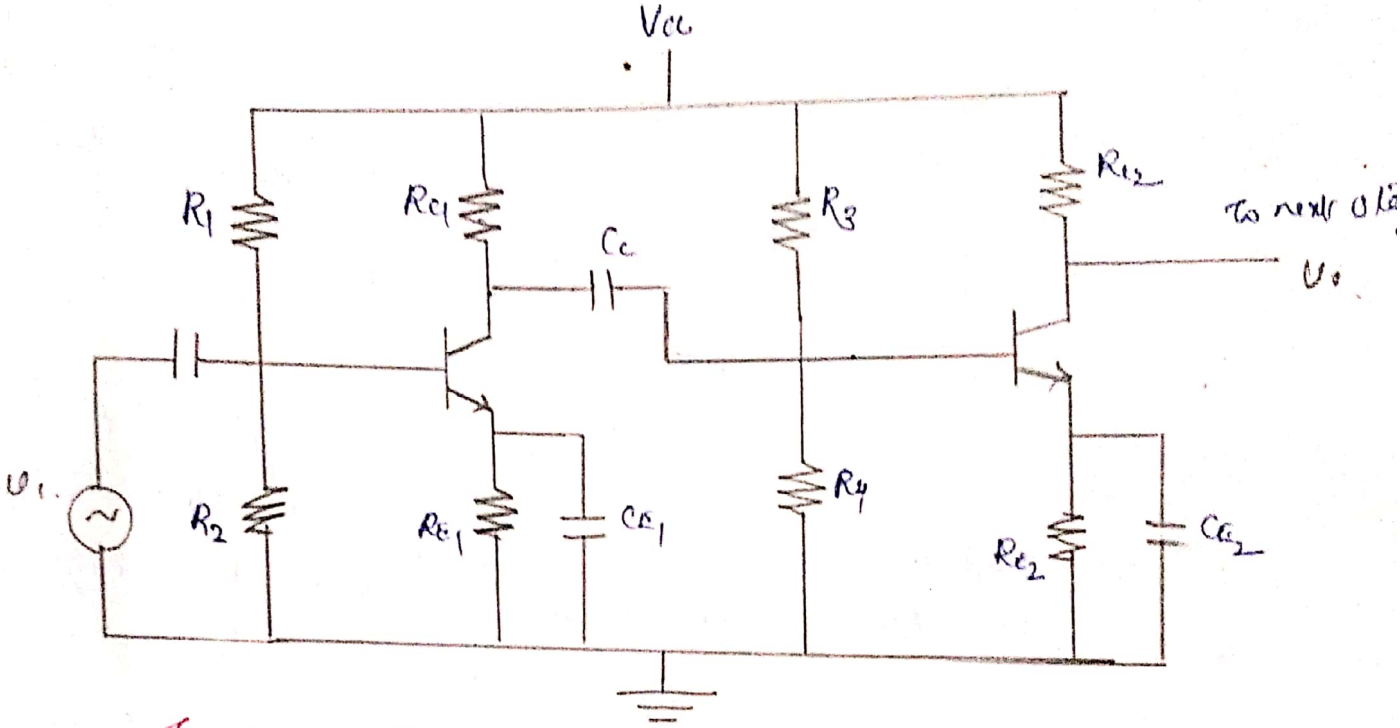
Over all gain $A = \frac{V_o}{V_s} = \frac{V_1}{V_s} \times \frac{V_2}{V_1} \times \frac{V_3}{V_2} \times \cdots \frac{V_o}{V_{n-1}}$

$$A = A_1 \times A_2 \times \cdots A_n$$

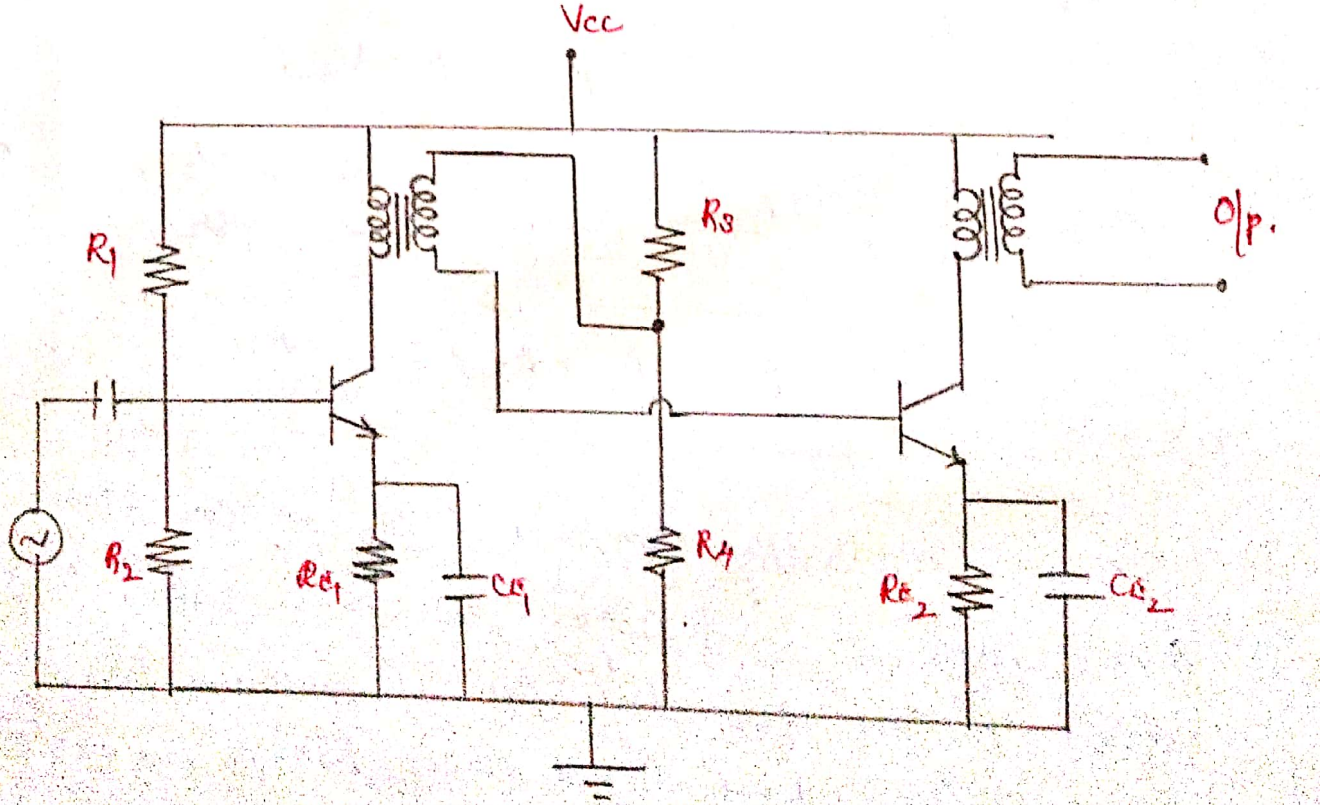
In a multistage amplifier o/p of one stage makes input of next stage. We must use a coupling network between two stages that a minimum loss of voltage occurs when signal passes through this network to next stage.

Various coupling schemes are
* Resistance capacitance [RC] coupling.
* Transformer coupling.
* Direct coupling.

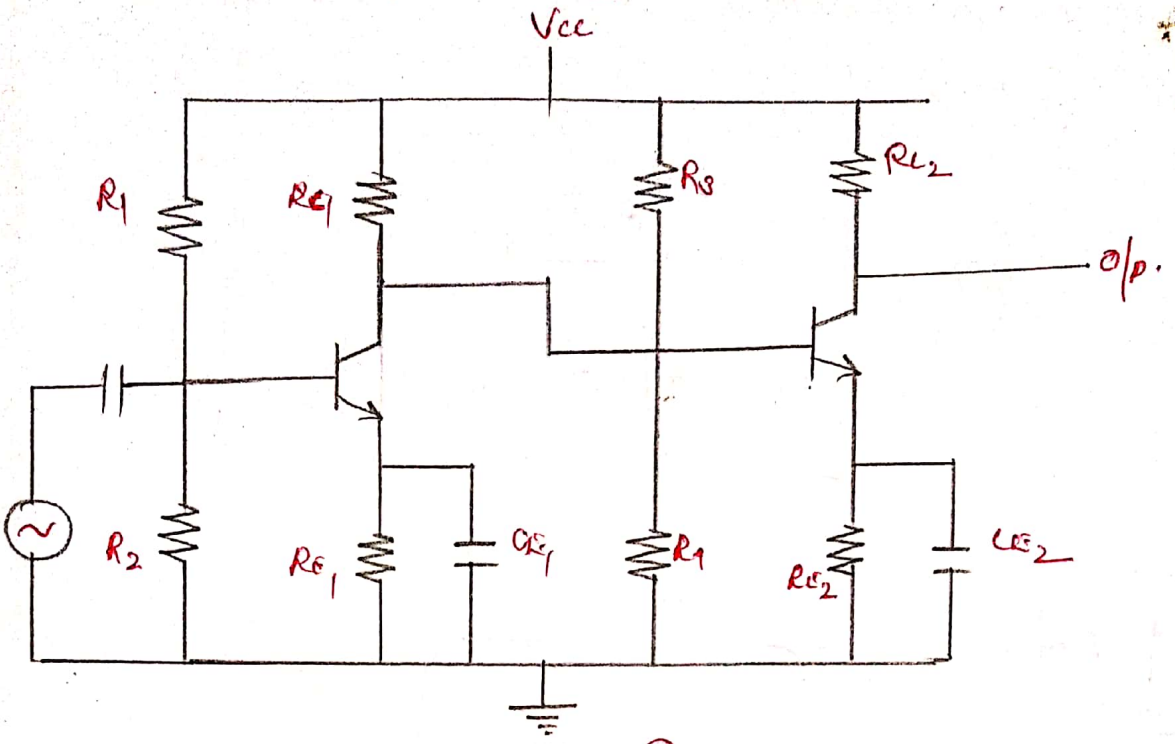
RC coupled Multistage Amplifier



Transformer Coupled Multistage amplifier.



Direct Coupled Amplifier:



Effect of Cascading on Gain and Bandwidth.

In a multistage amplifier a number of stages are cascaded to obtain higher value of voltage gain. If an 'n' stages are cascaded the overall midband voltage gain becomes

$$A_v' = (A_{vm})^n$$

where A_{vm} is the midband voltage gain of individual stage.

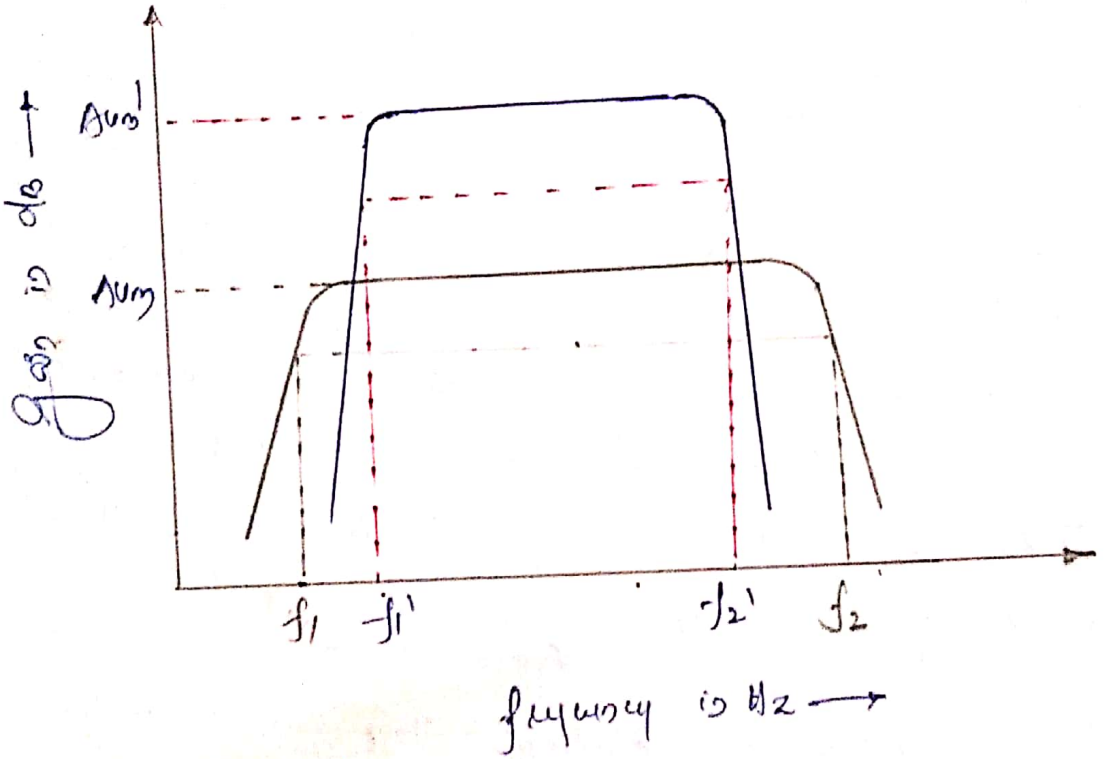
But Bandwidth of the amplifier does not remain the same. Bandwidth will decrease with cascading.

i) The upper cutoff frequency decreases and lower cutoff frequency increases. It happens because greater number of stages means greater number of capacitors in the circuit and each capacitor affects the frequency response adversely.

If f_1 & f_2 are lower and upper cut off frequencies of individual stage, the over all cut off frequencies are given by

$$f_1' = \frac{1}{\sqrt{2^{1/n} - 1}} \times f_1$$

$$f_2' = \sqrt{2^{1/n} - 1} \times f_2$$



: FEEDBACK AMPLIFIERS:

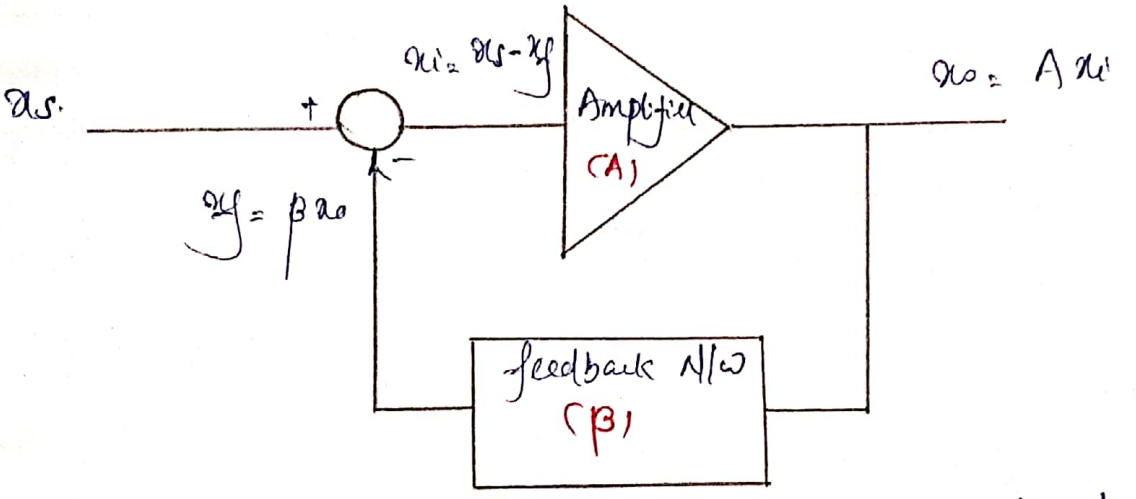
The voltage gain, input & output impedances and Bandwidth etc are few important characteristics of an amplifier. These parameters are more or less constant and for an amplifier and are required to be controlled. This is achieved by feedback.

Feedback is a technique in which a part of or a fraction of output is connected back to input

When the feedback applied is to increase the input signal, it is called Positive or Direct or Regenerative feedback

When the feedback is so applied as to decrease the input signal, it is called Negative or Inverse or Degenerative feedback.

Feedback in Amplifiers:



A feedback amplifier essentially consists of two parts
* An amplifier * A feedback Network.

The function of feedback N/w is to return a fraction of o/p energy (voltage or current) to input of amplifier usually it is made up of resistors, inductors or capacitors.

Negative feedback

$x_i = x_s - \beta x_o$.

$A = x_o / x_i$

$x_o = A x_i$

$= A[x_s - \beta x_o]$

$x_o[1 + A\beta] = A x_s$.

$$A_{Vf} = \frac{x_o}{x_s} = \frac{A}{1 + A\beta}.$$

Positive feedback

$x_i = x_s + \beta x_o$.

$A = x_o / x_i$

$x_o = A x_i$

$= A[x_s + \beta x_o]$

$x_o[1 - A\beta] = A x_s$.

$$A_{Vf} = \frac{x_o}{x_s} = \frac{A}{1 - A\beta}.$$

Effect of Negative Feedback on Amplifier.

Even though the amplifier gain is reduced with negative feedback, negative feedback improves the performance of amplifier from various other points of view.

The advantages of -ve feedback are

* It improves the stability of amplifier gain.
* It reduces the distortion and noise.
* It increases input impedance
* It reduces output impedance
* It increases Bandwidth

Gain Stability

gain with -ve feedback

$$A_{Vf} = \frac{A}{1+A\beta} \qquad A\beta >> 1$$

$$\therefore A_{Vf} = \frac{A}{A\beta} = \frac{1}{\beta}.$$

Since β is the feedback gain which depends only on passive components (such as resistors which are fixed; the gain with feedback is almost stable.

Reduces Distortion or Noise

If 'D' is the distortion without feedback & D_f, the distortion with feedback then

$$D_f = \frac{D}{1+A\beta}.$$

The distortion is reduced by the same factor as the gain.

Increase in input impedance

Z_i = input impedance without feedback

Z_{if} = input impedance with feedback

Then

$$Z_{if} = Z_i(1+A\beta)$$

Decrease in output impedance

Z_o = Output impedance without feedback

Z_{of} = Output impedance with feedback

Then

$$Z_{of} = \frac{Z_o}{1+A\beta}$$

Increase in Bandwidth

BW = Bandwidth without feedback

BW_f = Bandwidth with feedback

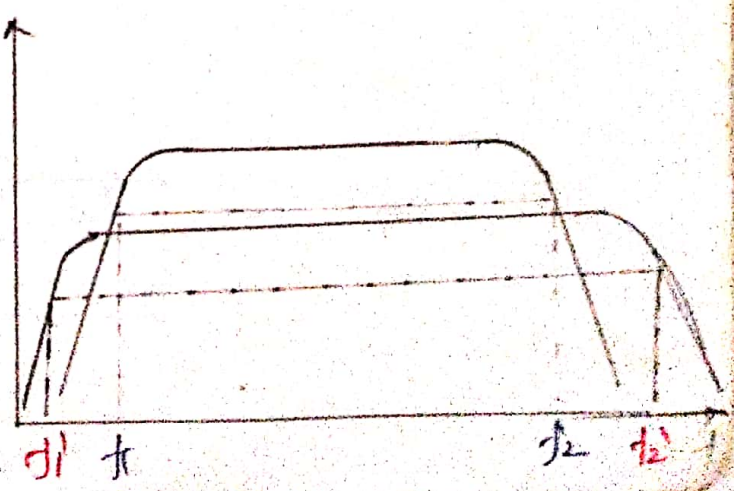
$$BW_f = BW(1+A\beta)$$

Negative feedback Reduces the lower cutoff frequency and Increases upper cutoff frequency

$$f_1' = \frac{f_1}{1+A\beta} \quad ; \text{lower cut off freq}$$

$$f_2' = f_2(1+A\beta) \quad ; \text{upper cut off freq}$$

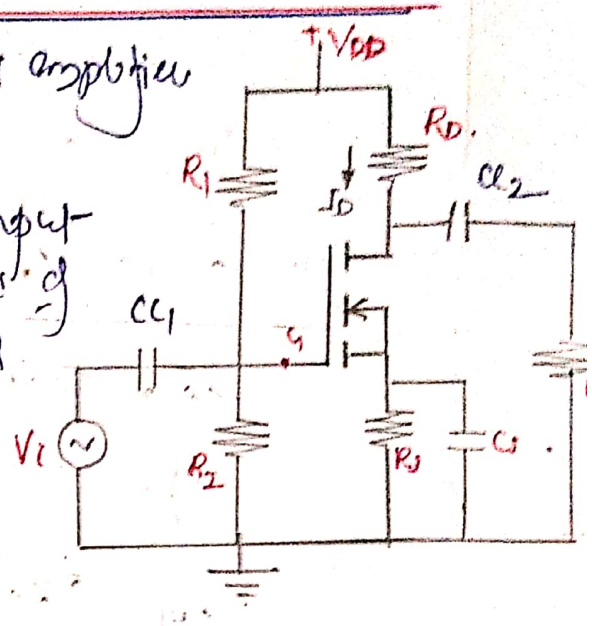
$$BW = f_2' - f_1'$$



MOSFET AMPLIFIERS

Common Source Amplifier Using E-MOSFET

Figure shows a CS MOSFET amplifier where voltage divider bias configuration is used. The input signal is applied to the Gate of amplifier FET. Because of insulated gate; current $I_G = 0$.



CC_1 & CC_2 are coupling capacitors & C_S is the by-pass capacitor.

the equation for Drain current for an enhancement MOSFET is $I_D = K[V_{GS} - V_{GS(TH)}]^2$

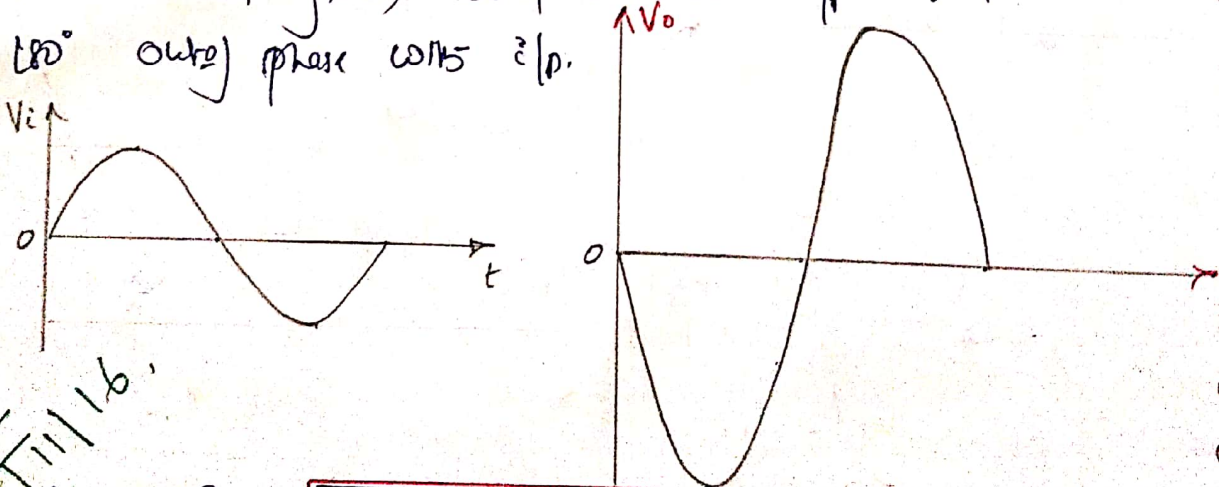
V_{GS} = Gate to Source voltage

$V_{GS(TH)}$ = Gate to source threshold voltage in which channel creates.

The o/p voltage will be obtained from Drain end of amplifier.

$$V_o = V_{DD} - I_D R_D.$$

CC_2 will block the dc component and final o/p will be collected from local resistor. o/p signal will be 180° out of phase with i/p.



Voltage gain

$$A_V = \frac{V_o}{V_i} = -g_m (R_d \parallel R_D)$$

MODULE 4

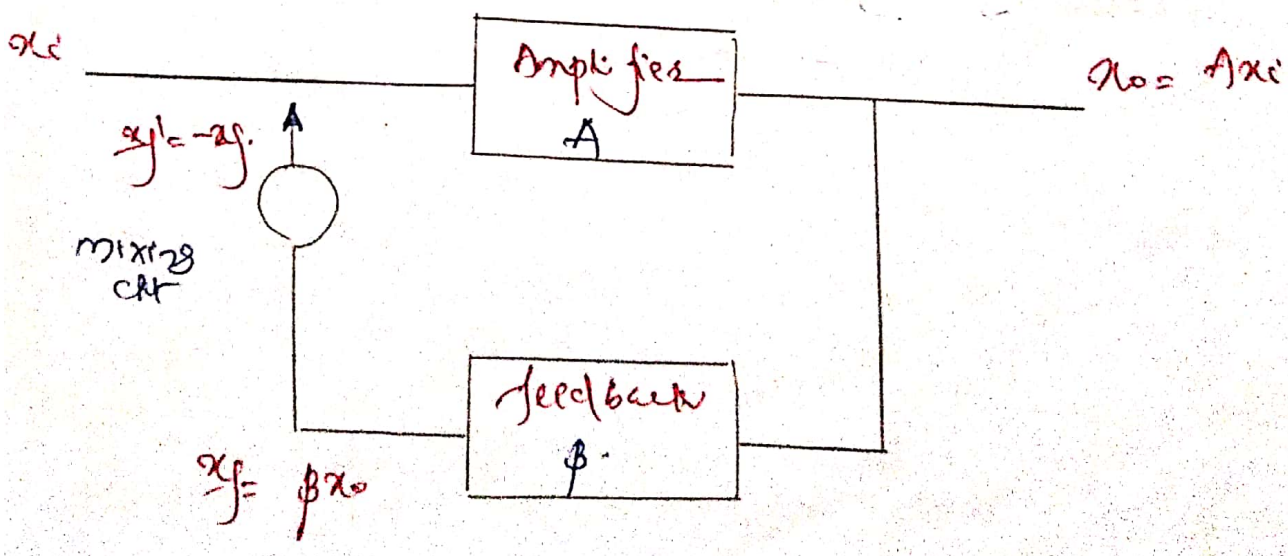
MODULE IV

—: OSCILLATORS :—

Classification

- Oscillators
  - Sinusoidal
    - Low freq. (RF)
      - RC phase shift oscillator
      - Wein Bridge Oscillator
    - High freq. (RF)
      - LC osc
        - Hartley osc
        - Colpitts osc
      - Crystal osc
  - Non Sinusoidal
    - Square wave (M.V)
      - Astable M.V
      - Monostable M.V
      - Bistable M.V.
    - Triangular wave

Principle of Oscillators or Criterion for Oscillators



Here amplifier provides an o/p signal $x_o = Ax_i$

-feedback signal $x_f = \beta x_o = -A\beta x_i$

from figure o/p of mixing ckt $= -x_f$.

$$\text{loop gain} = \frac{x_{f1}}{x_i} = \frac{-x_f}{x_i} = \frac{-A\beta x_i}{x_i}$$

$$= -A\beta$$

If $x_{f1} = x_i$ we can connect x_{f1} as input of ckt instead of x_i

For that condition to be satisfied is $-A\beta = 1$

i.e.

$$|A\beta| = 1$$

$$\angle A\beta = 0^\circ \text{ or } 360^\circ.$$

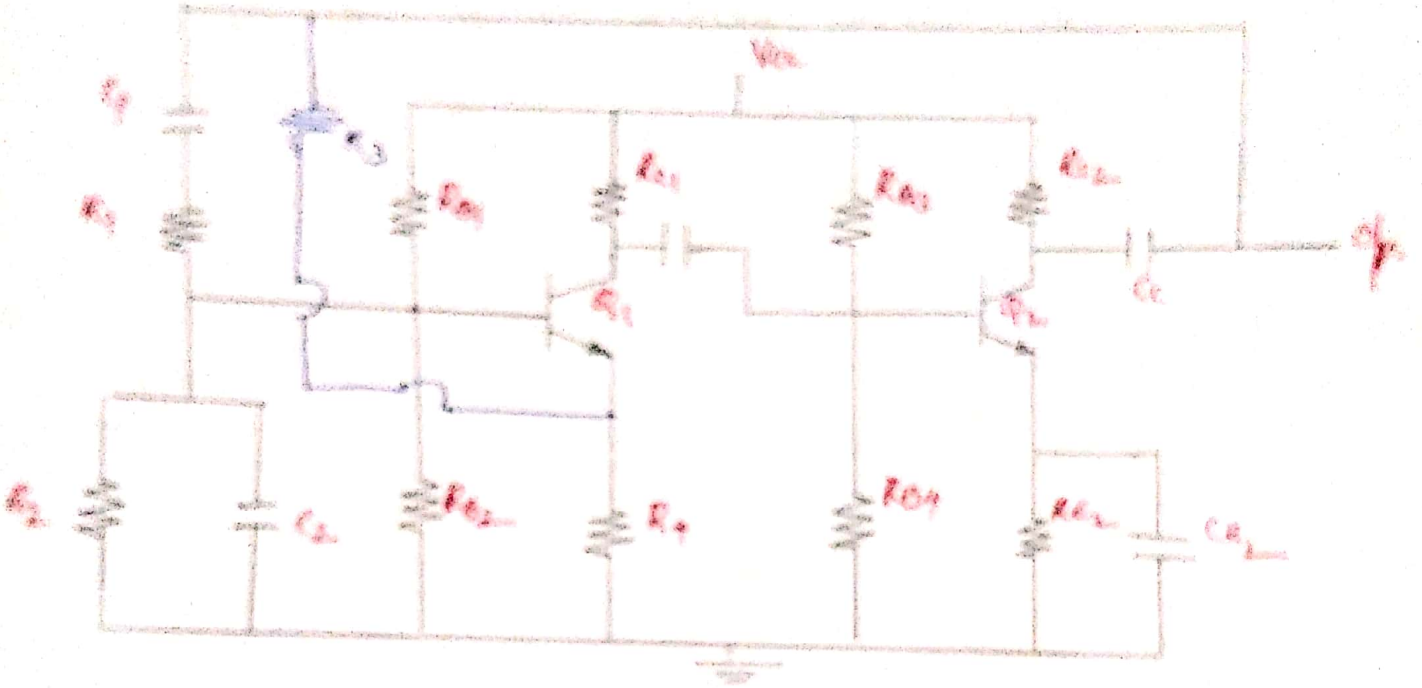
This is called Barkhausen's Criteria.

Oscillators are classified in terms of their output waveforms; freq. range; components or ckt configuration.

If output waveform is sinusoidal it is called Sinusoidal Oscillator otherwise called Relaxation Oscillators which include square, rectangular and Sawtooth waveforms.

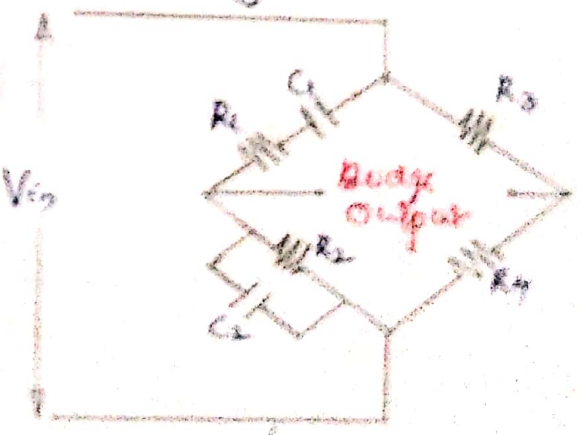
Wien Bridge Oscillator

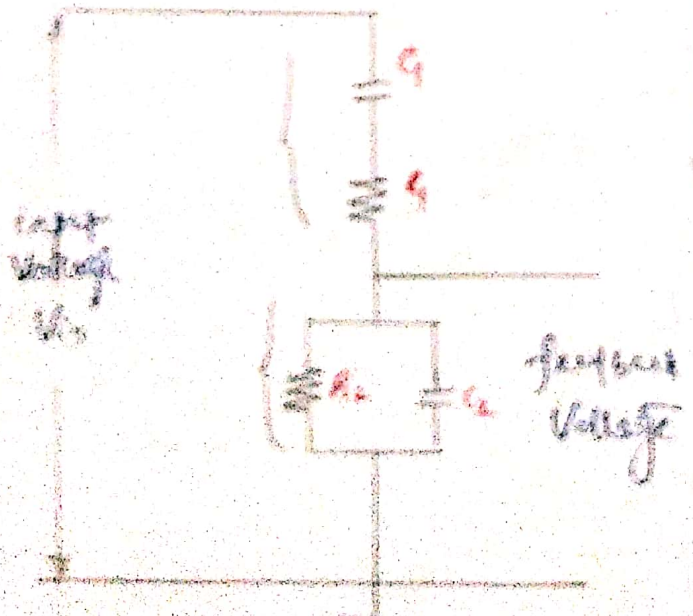
Wien bridge oscillator uses a Wien bridge as frequency selective network in the basic feedback loop. The bridge consists of R_1 & C_1 in series arm and R_2 & C_2 in parallel arm. The oscillation frequency



& has less feedback the feedback generally oscillates and the feedback gives stability

Analysis:





From figure it can be noted that V_{in} is actually the o/p voltage of amplifier, V_{out} & voltage across R_2C_2 act as feedback voltage V_f.

Gain of feedback n/w $\beta = \frac{V_f}{V_{in}}$

Let Z_1 be impedance of series connected of R_1C_1

Z_2 effective impedance of II^{el} n/w R_2C_2

$$\therefore V_f = \frac{Z_2}{Z_1 + Z_2} \times V_{in}$$

$$\beta = \frac{Z_2}{Z_1 + Z_2} \quad \text{----- 1)}$$

Now $Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1 + j\omega C_1 R_1}{j\omega C_1}$

$$Z_2 = \frac{R_2 \cdot \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} = \frac{R_2}{1 + j\omega C_2 R_2}$$

$$\therefore \beta = \frac{\frac{R_2}{1 + j\omega C_2 R_2}}{\left[\frac{1 + j\omega C_1 R_1}{j\omega C_1}\right] + \left[\frac{R_2}{1 + j\omega C_2 R_2}\right]}$$

Sub: $S = j\omega$

$$\beta = \frac{\frac{R_2}{1 + SR_2C_2}}{\frac{1 + SR_1C_1}{SC_1} + \frac{R_2}{1 + SR_2C_2}}$$

$$\beta = \frac{SC_1R_2}{(1 + SR_1C_1)(1 + SR_2C_2) + SR_2C_1}$$

$$= \frac{SC_1R_2}{1 + SR_2C_2 + SR_1C_1 + S^2R_1R_2C_1C_2 + SR_2C_1}$$

$$\beta = \frac{sC_1R_2}{1 + s[R_1C_1 + R_2C_2] + s^2R_1R_2C_1C_2 + sR_2C_1}$$

$$= \frac{sC_1R_2}{1 + s[R_1C_1 + R_2C_2 + R_2C_1] + s^2[R_1R_2C_1C_2]}$$

Sub. $s = j\omega$ & $s^2 = -\omega^2$

$$\beta = \frac{j\omega C_1R_2}{1 + j\omega[R_1C_1 + R_2C_2 + R_2C_1] - \omega^2R_1R_2C_1C_2}$$

$$= \frac{j\omega C_1R_2}{1 - \omega^2R_1R_2C_1C_2 + j\omega[R_1R_1 + R_2C_2 + R_2C_1]}.$$

Multiply with complex conjugate of D_2 on N_2 & D_2.

$$\therefore \beta = \frac{j\omega R_1R_2[(1 - \omega^2R_1R_2C_1C_2) - j\omega(R_1C_1 + R_2C_2 + R_2C_1)]}{(1 - \omega^2R_1R_2C_1C_2)^2 + \omega^2(R_1C_1 + R_2C_2 + R_1C_1)^2}$$

Equate imaginary part to zero.

$$j\omega C_1R_2(1 - \omega^2R_1R_2C_1C_2) = 0.$$

$$\omega^2R_1R_2C_1C_2 = 1$$

$$\omega^2 = \frac{1}{R_1R_2C_1C_2} \qquad \omega = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

$$\therefore f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \quad ; \text{ if } R_1 = R_2 = R \; ; \; C_1 = C_2 = C$$

$$f = \frac{1}{2\pi RC}.$$

Now feedback factor

$$\beta = \frac{\omega^2RC(3RC) + j\omega CR(1 - \omega^2R^2C^2)}{(1 - \omega^2R^2C^2)^2 + \omega^2(3RC)^2}$$

Equating Real part

$$\beta = \frac{3}{6+9} = 3/9 = \underline{1/3}$$

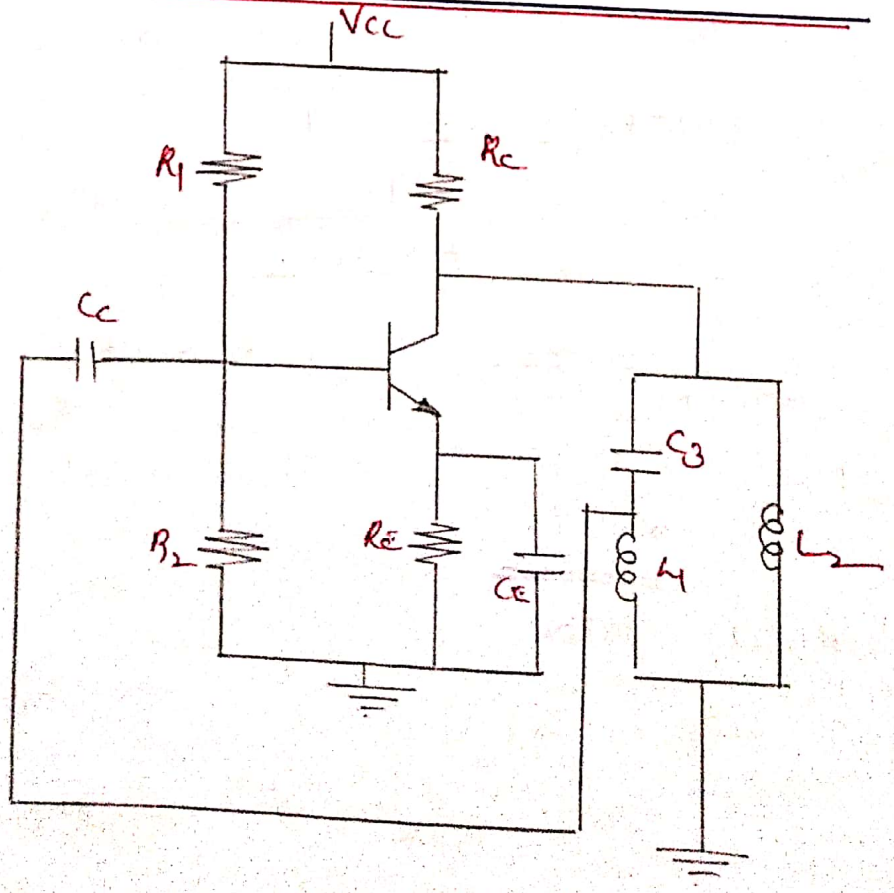
For Sustained Oscillations $|A\beta| \geq 1$

$$A \geq 3$$

Amplitude Stabilization.

For Sustained Oscillations amplifier gain $A \geq 3$, the gain of amplifier should not be too large as it will distort the o/p waveform.
∴ amplifier gain should be controlled.
This is achieved by introducing -ve feedback by keeping resistor R_4 in emitter of Q_1 unbypassed. This introduces current series -feedback. This process of gain reduction using -ve feedback is known as amplitude stabilization.

HARTLEY OSCILLATOR:



Hartely Oscillator is a High frequency (RF) Oscillator which uses two inductors & a capacitor in the feedback N/w which decides the frequency of Oscillation.

For sustained oscillations the condition to be satisfied is $X_1 + X_2 + X_3 = 0$.

where $X_1 = \omega L_1$; $X_2 = \omega L_2$ & $X_3 = \frac{-1}{\omega C_3}$.

$$\therefore \quad \omega L_1 + \omega L_2 = \frac{1}{\omega C_3}$$

$$\omega [L_1 + L_2] = \frac{1}{\omega C_3}$$

$$\omega^2 = \frac{1}{C_3 (L_1 + L_2)}$$

$$\omega = \frac{1}{\sqrt{(L_1 + L_2) C_3}}$$

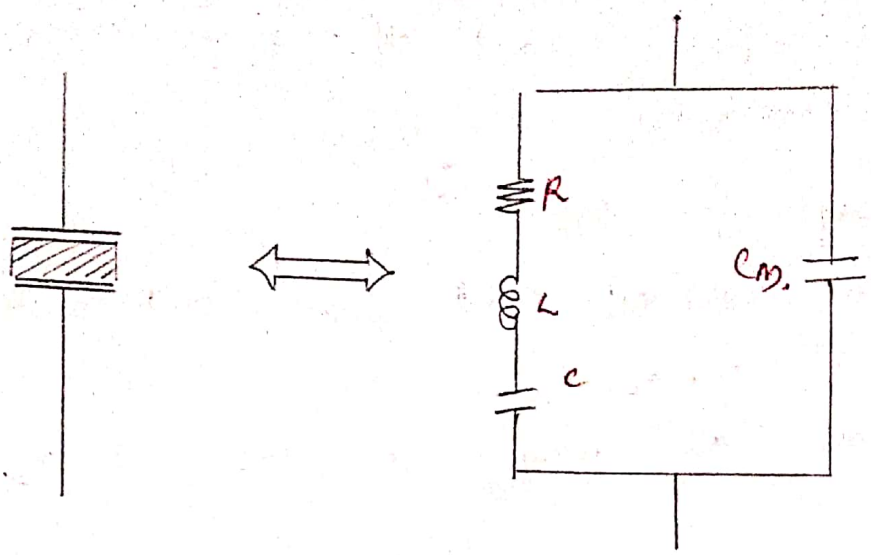
$$f = \frac{1}{2\pi \sqrt{(L_1 + L_2) C_3}}$$

$$\boxed{f = \frac{1}{2\pi \sqrt{(L_1 + L_2) C_3}}}$$

· CRYSTAL OSCILLATORS:

A crystal oscillator is basically a tuned ckt oscillator using piezo electric crystal as resonant tank ckt. Crystal has greater stability in holding constant frequency to which it is originally cut to operate.

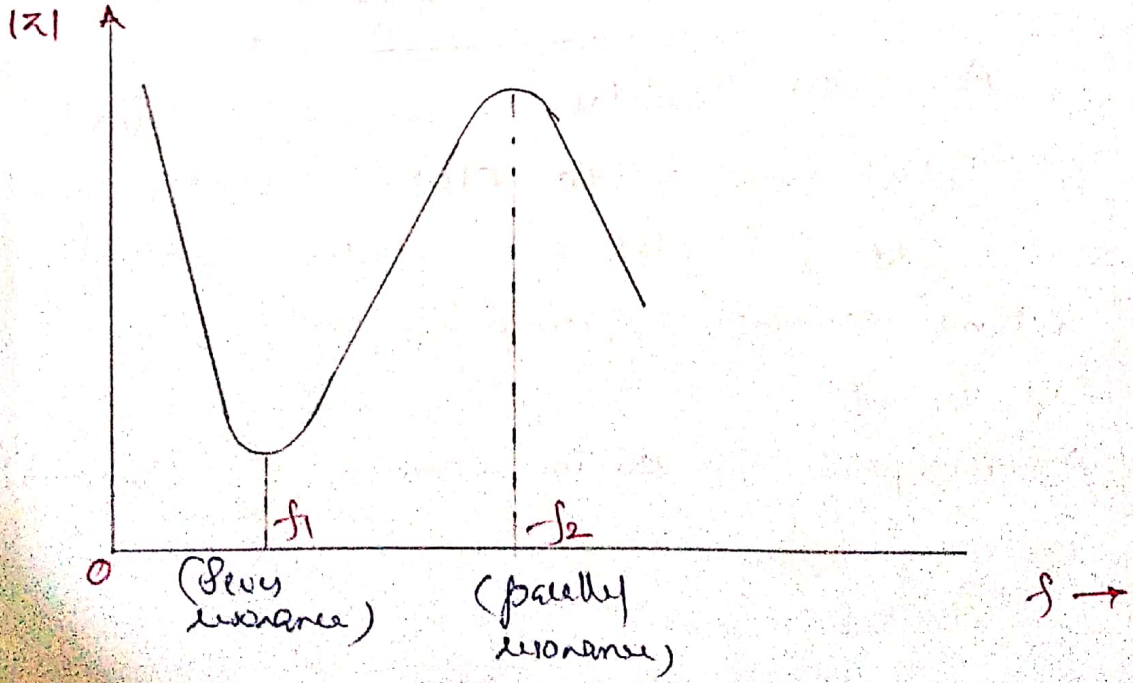
Main application are in communication transmitters & receivers.



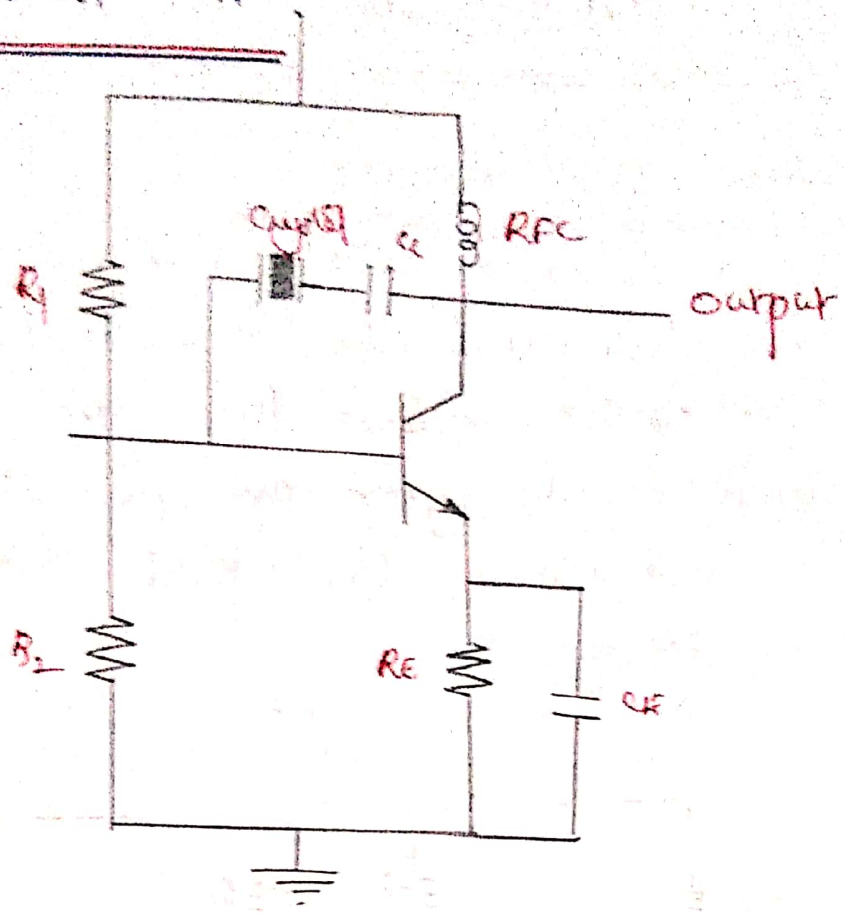
Electrical equivalent ckt of a crystal

The crystal can have two resonant frequencies. One resonant condition occurs when reactances of series RLC leg are equal (and opposite). For this condition series impedance is very low.

The second resonant condition occurs at a higher frequency when reactance of series resonant leg equals reactance of capacitor C_M. At this frequency crystal offers a very high impedance to external ckt.



Series Resonant ckt



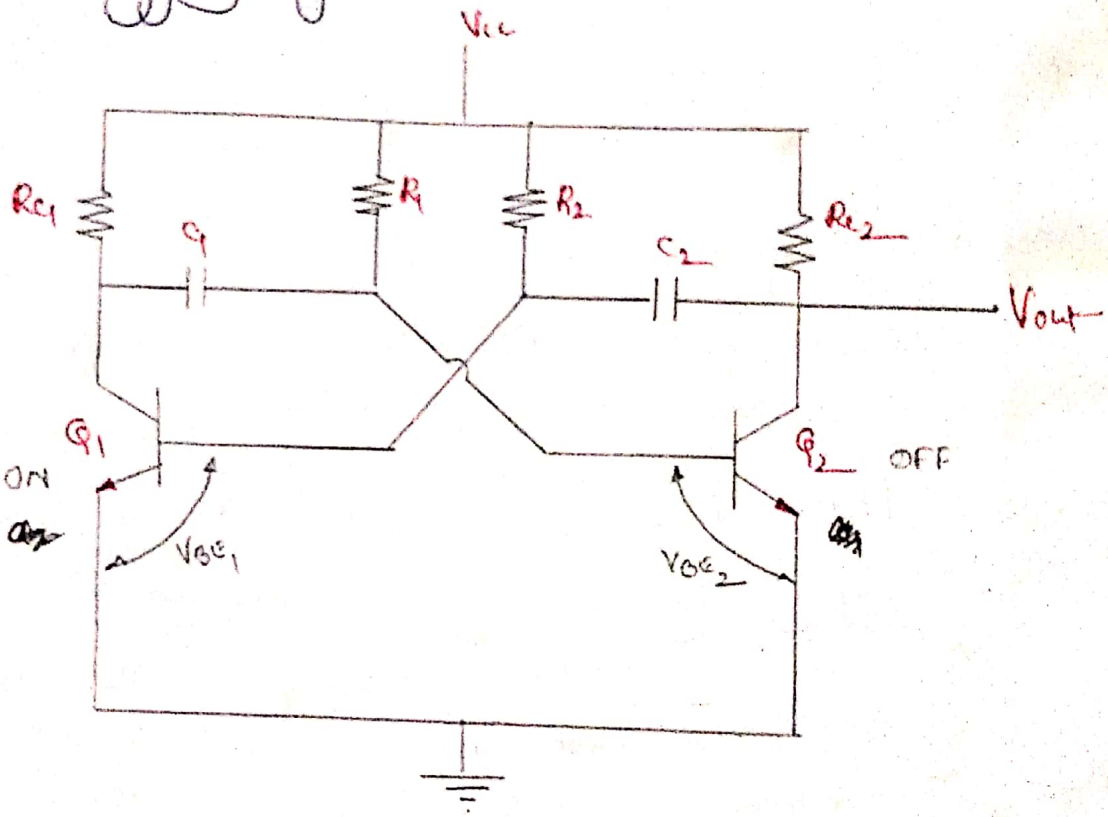
Here Crystal is connected as series element in a feedback path. At series resonant mode impedance is smallest & amount of feedback (+ve) is largest.

Here - RFC coil provides dc bias while decoupling any ac signal from affecting o/p signal. The oscillator ckt frequency of oscillation is set by series resonant frequency of crystal.

Multivibrators

Astable Multivibrators:

It is also called free running multivibrator. It has no stable states. The two states of operation of MV are quasi stable (temporary) states. The MV thus you make successive transitions from one quasi stable state to another after a predetermined time interval without the aid of external triggering signal.



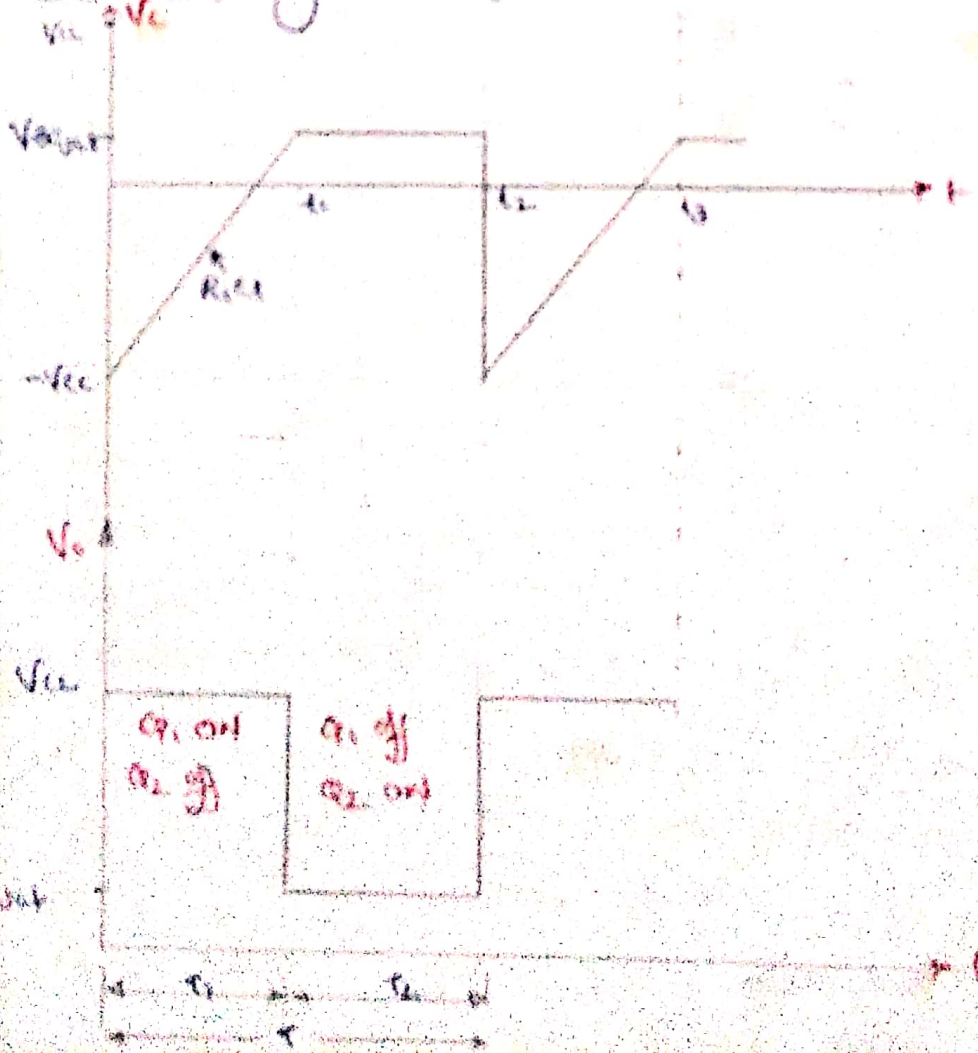
When power is first applied to the circuit both transistors starts conducting. Because of parameter variations one of the transistors conducts more than other.

Let us assume Q_1 conducts more than Q_2, resulting less voltage. This causes collector voltage of Q_1 drops rapidly than Q_2. resulting less voltage fed to base of Q_2 through the capacitor C_1 and drives it to cutoff. As a result of this collector

voltage of Q_2 rises towards V_{cc}. When it goes beyond the base of Q_1 and drives it to saturation.

As soon as Q_1 starts conducting capacitor C_1 charges towards V_{cc} through R_1. When the voltage across C_1 rises beyond $V_{BE(on)}$ of Q_2 it begins to conduct. As Q_2 is conducting, now its collector voltage drops to low voltage that is applied to the base of Q_1 through capacitor C_2 and makes it off.

Now since Q_2 is conducting capacitor C_2 charges towards V_{cc} through R_2. When voltage across C_2 rises beyond $V_{BE(on)}$ of Q_1, Q_1 starts conducting and its collector voltage drops. This low voltage makes Q_2 off. and this cycle repeats. Since the taken up from the collector of one of the transistor can get a square wave.



Design eqs for

$T_1 = 0.693 R_1 C_1$

$T_2 = 0.693 R_2 C_2$

total time period $T = T_1 + T_2$

$= 0.693 (R_1 C_1 + R_2 C_2)$

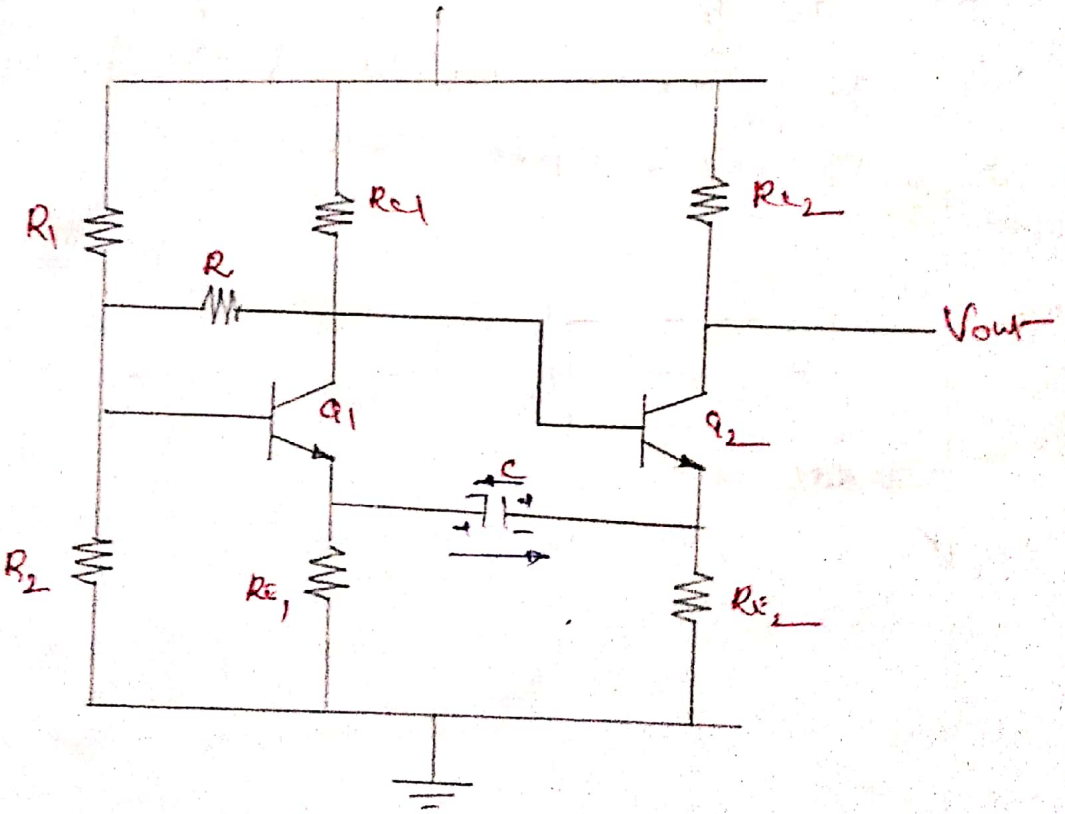
cons $R_1 = R_2 = R$

$C_1 = C_2 = C$

$T = 2 \times 0.693 RC$

$T = 1.386 RC$

EMITTER COUPLED AMV



In emitter coupled AMV capacitor C is connected b/w emitters of two transistors.

Here we assume transistor Q_2 is conducting first. The current through R_{C_2} makes collector voltage to drop. This drop is followed by R_E, which follows

Analysis: The emitter voltage keeps Q_1 off. Also C begins to charge and emitter voltage of Q_1 starts falling. When capacitor voltage reaches a particular level it causes Q_1 to conduct. This collector voltage drops when Q_1 starts conducting, the collector voltage of Q_1 is fed to base which keeps Q_2 in cut off.

Also C charges to reverse direction and it goes into a level slightly emitter voltage of Q_1 falls and forces it to conduct. Also Q_1 conducts drop across R_E couples to emitter of Q_1 & makes it off.

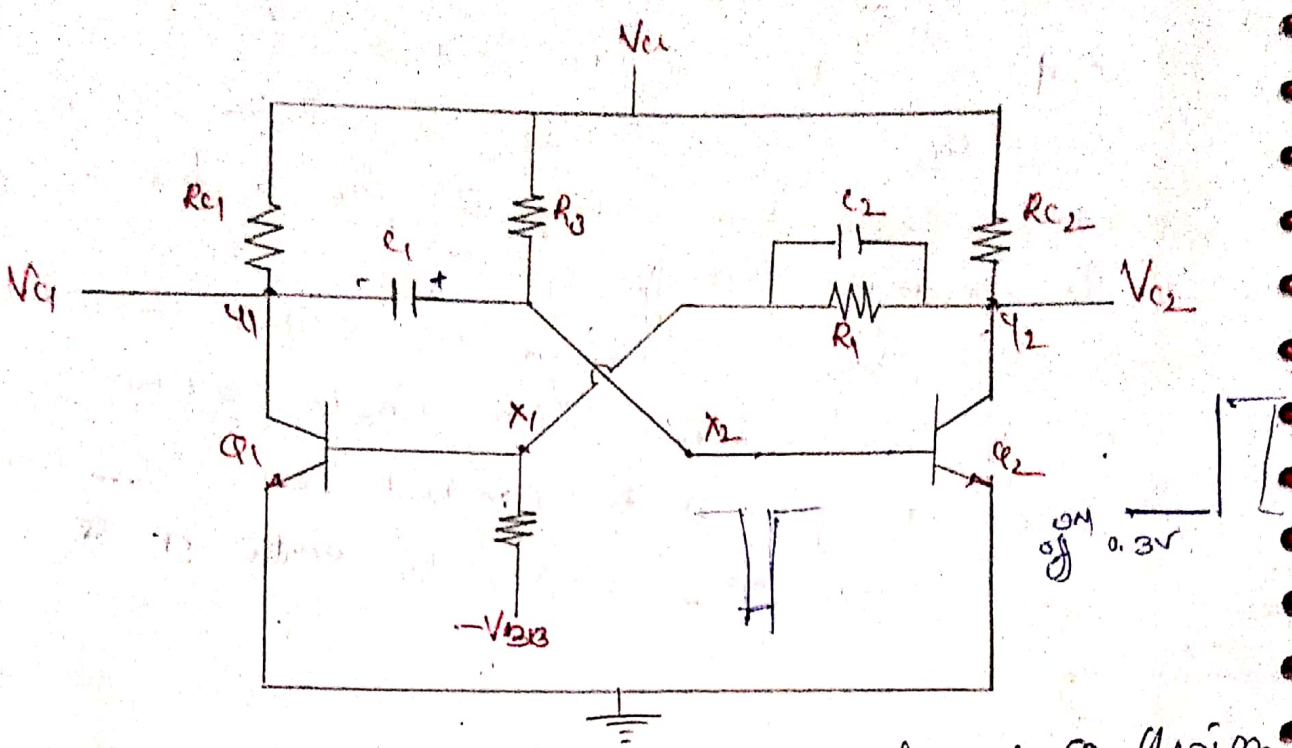
Monostable M.V.

A mono stable M.V has only one stable state and other being quasi stable state. When an external triggering pulse is applied to a particular point in the circuit it causes a transition from one stable state to another & quasi state. The circuit stays in quasi state for a predetermined time and comes back to stable state automatically. This ckt is also known as One-shot, Single shot, Single cycle or One-Vibrator.

Collector coupled MMV.

In this mmv the collector of Q_2 is coupled to base of Q_1 through R & C_2. Where C_2 is speed up capacitor. How the coupling from collector of Q_1 to base of Q_2 has been replaced by

a capacitive coupling through C_1. The -ve supply voltage exists, resistance R_2 keeps Q_1 off

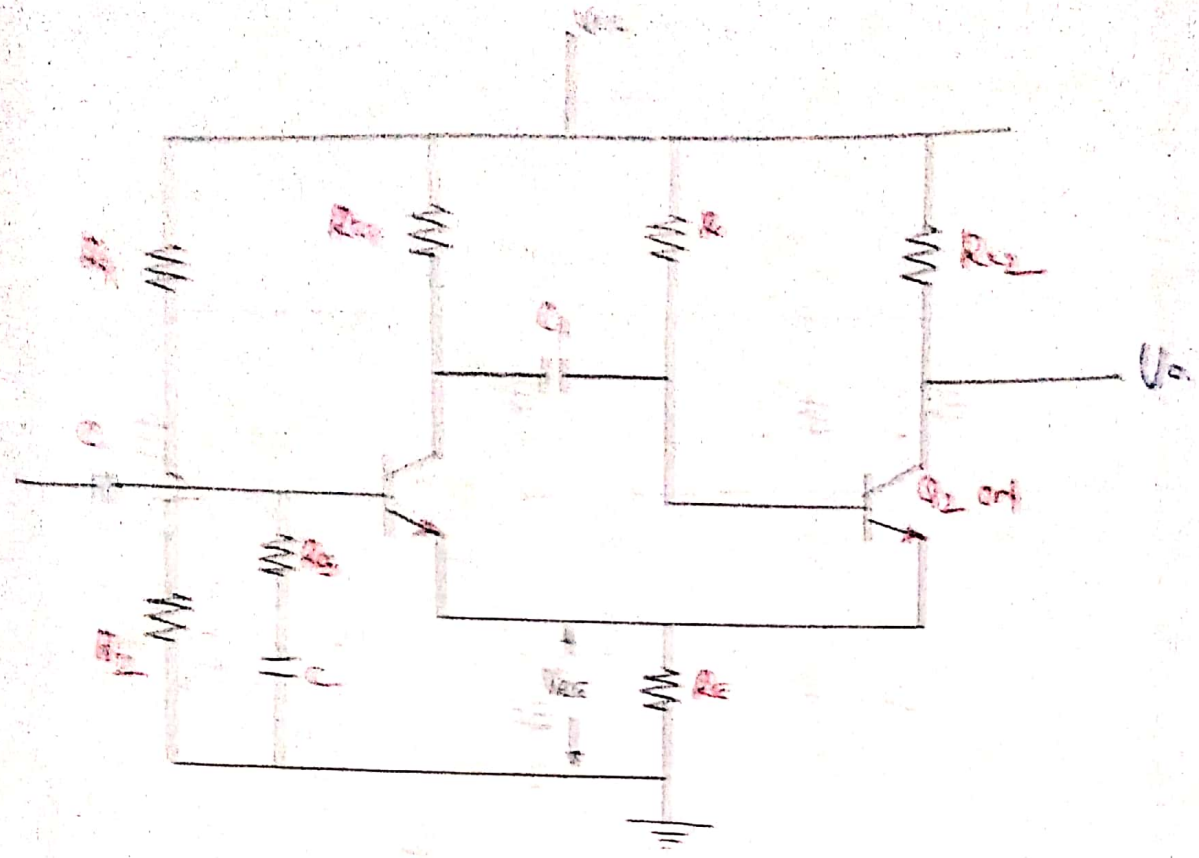


Here o/p of Q_2 is connected to base of Q_1 through a emitter attenuator in which C_2 is commutating capacitor. The ckt parameters have been adjusted properly so that MV sets its stable state with Q_1 off and Q_2 ON. MV make a transition by the application of -ve triggered pulse at base of Q_2 or collector of Q_1

The -ve pulse applied at base of Q_2 driving Q_2 completely off. The voltage at collector of Q_2 now rises to Vcc & Q_1 now comes into saturation. C starts charging towards Vcc through R_3. when voltage across C_1 rises above $V_{BE_{ON}}$ of Q_2 it again conducts & comes back to stable state.

Emitter Coupled MMV

An alternate form of ckt that is shown in figure Here the feedback is given through a common resistor RE.



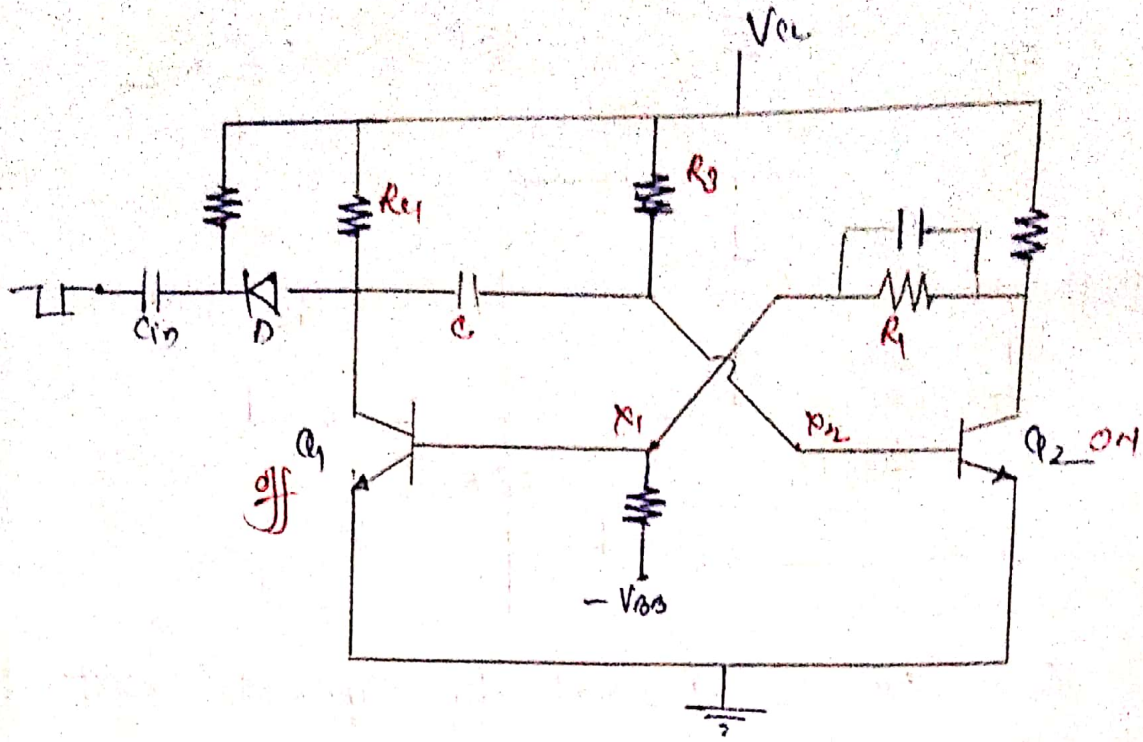
This circuit is designed for operating such Q_2 normally on and Q_2 off. This is called stable

As Q_2 conducting large current R_E is large enough to provide a -ve bias at base of Q_1. Thus Q_1 stays cut stable.

Now a +ve trigger pulse with sufficient amplitude is given at the base of Q_1 makes it ON when Q_1 starts conducting its collector voltage drops. This reduced voltage is applied to the base of Q_2 through C_1 and makes Q_2 off.

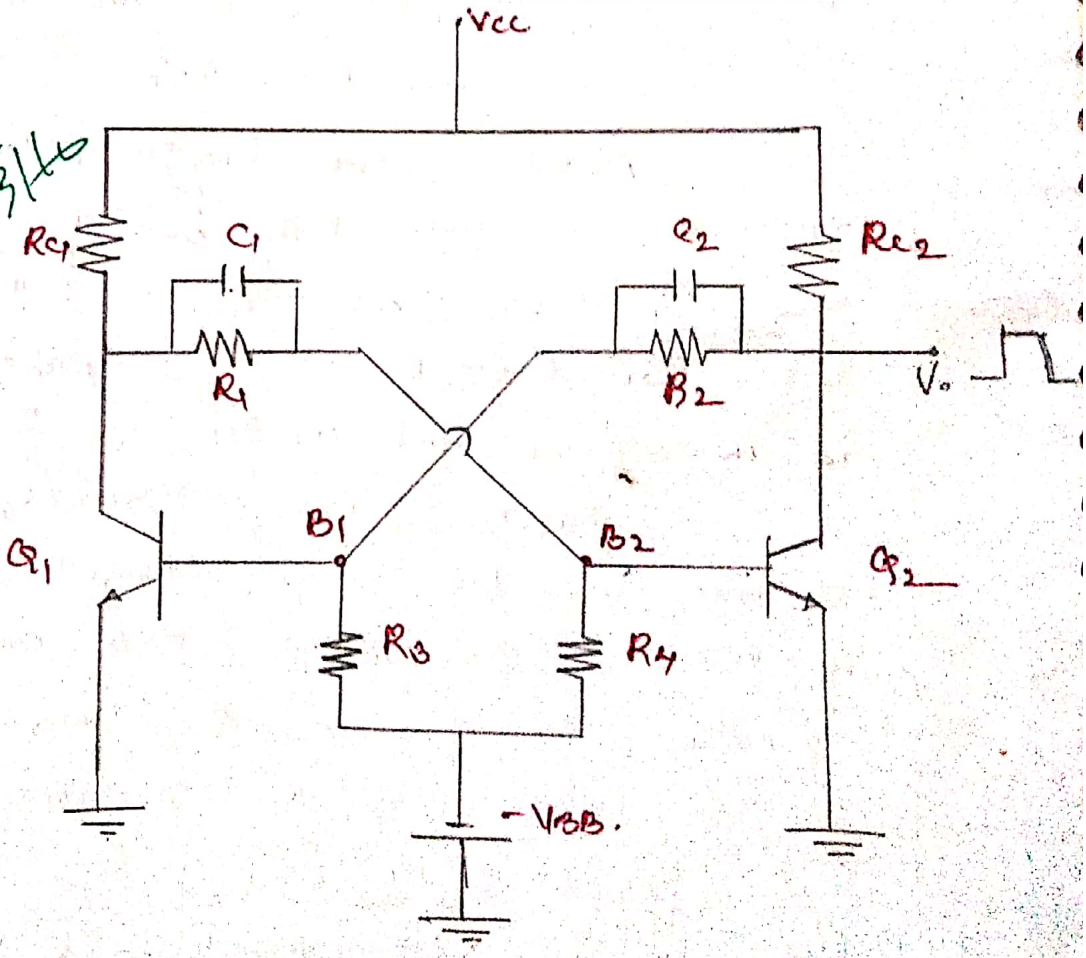
Now C_1 charges towards V_{cc} through R_{c1} and Q_1. As C_1 gets charged base potential of Q_2 rises. As the voltage at the base of Q_2 becomes sufficiently large it conducts. When Q_2 starts conducting large current R_E increases and reduces the bias applied at the base of Q_1. Finally it becomes off. Thus the circuit reverts back to its original stable state.

Triggering of MMV.



: BISTABLE MULTIVIBRATOR:

Verified
19/9/16

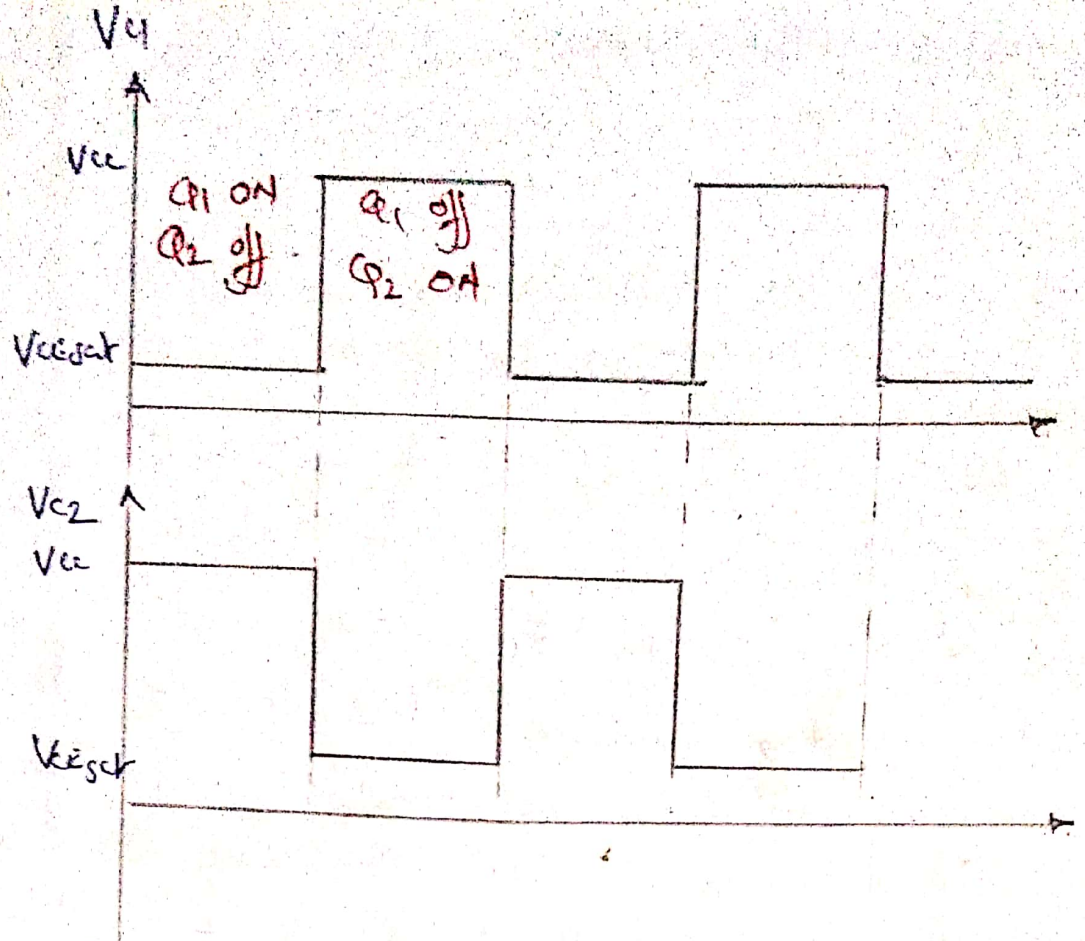


It is also called Flip flop or Binary. It has two stable states. A trigger pulse applied to the circuit will cause it to switch from one state to another. Another pulse is then required to switch the ckt back to its original state.

In the ckt the o/p of Q_2 is coupled to base of Q_1 through R_2. Similarly o/p of Q_1 is coupled to Q_2 through R_1. When a trigger pulse is applied, transition from one state to other should occur instantaneously. The conduction transfers from one transistor to other should be small as possible. The main purpose of C_1 & C_2 is to improve the switching characteristics of ckt by passing high frequency components of square wave pulse. This allows fast rise and fall times. C_1 & C_2 are then called commutating capacitors or speed up capacitors.

When switched on one transistor is driven into saturation & other into cutoff. Let us assume Q_1 is ON & Q_2 off. It is the stable state and will remain in that state till the trigger pulse is applied from outside.

A +ve trigger pulse applied at the base of Q_2 will increase forward bias & thereby lowering Q_2 ON. and thereby decrease collector voltage. The fall in collector voltage is coupled to base of Q_1 and keeps it to off. The ckt is in its second stable state and remains so till a +ve trigger pulse applied at base of Q_1.



Applications

* A bistable MV is used as memory elements in shift register counters & so on.
* It can used as a frequency divider.

Assignment:

Triggering methods for Bistable.

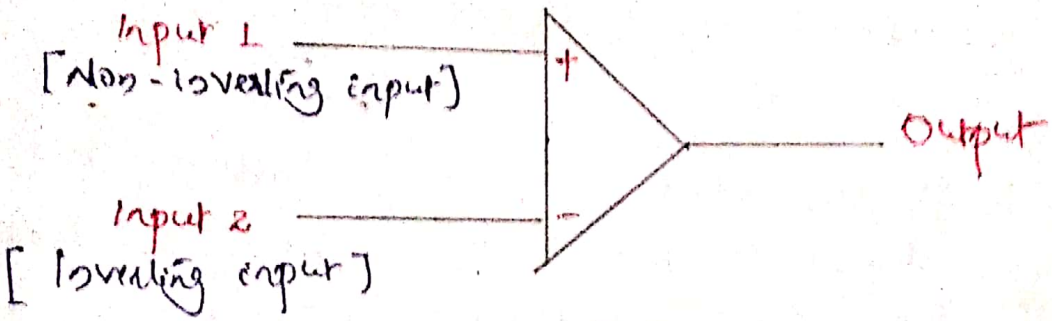
6/11/16

MODULE 5

MODULE V

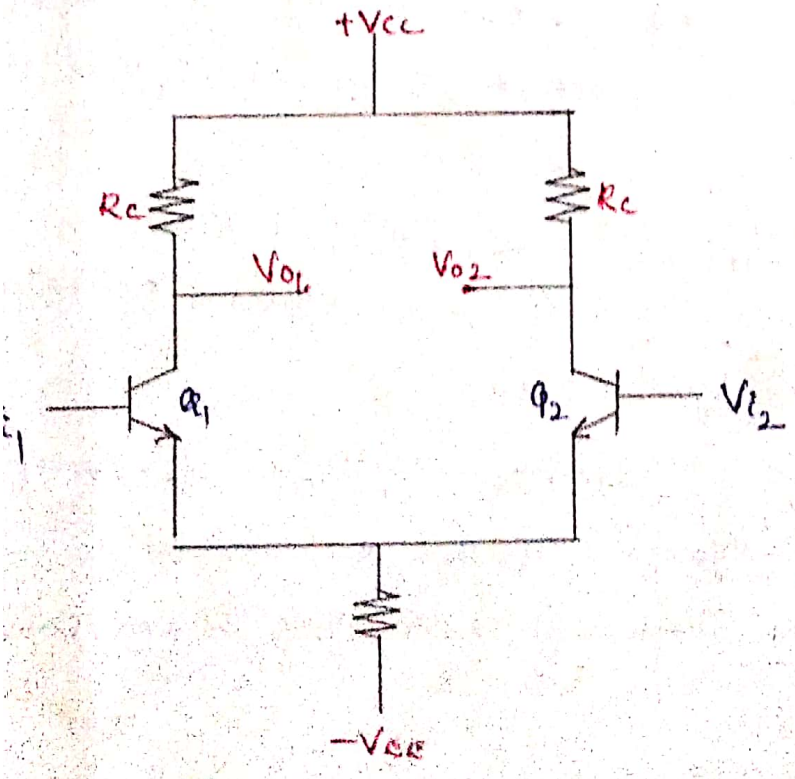
: OPERATIONAL AMPLIFIERS :

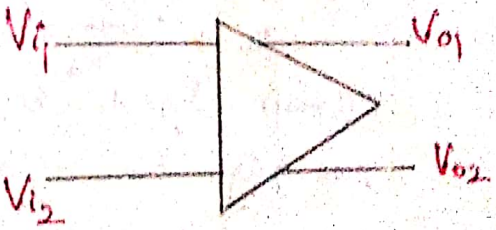
An Operational amplifier or Op-amp is a very high-gain differential amplifier with high input impedance and low o/p impedance. Typical use of Operational Amplifiers are amplifiers, oscillators and filter circuits also in many instrumentation circuits.



Basic Op-amp.

Differential Amplifier





Basic Differential Amplifier ckt

A basic differential amplifier has two identical input and two identical outputs and emitter are connected together.

A differential amplifier a number of input signal combinations are possible.

1. If an input signal is applied to either input with other input connected to ground, the operation is referred as Single-ended.
2. If two opposite polarity input signals are applied, the operation is referred as Double ended.
3. If the same input is applied to both inputs, the operation is called Common mode.

In Single ended operation, a single input is applied however due to common emitter connection, the input signal operates both transistors; resulting in output from both collectors.

In double ended operation two input signals are applied, the difference of the inputs resulting in outputs from both collectors due to difference of signals applied to both inputs.

In common-mode the common signal results in opposite signals at each collector these signals cancelling resulting in output signal zero

The main feature of differential amplifier is very large gain when opposite signals are applied to inputs compared to very small gain resulting from common inputs.

The ratio of difference gain to common gain is called common mode rejection ratio (CMRR).

Characteristics of Op-amp

1. Input offset voltage :
   This is the voltage that must be applied between two input terminals of an op-amp to null the o/p.

2. Input offset current :
   It is the difference between two input currents. (current to inverting & non inverting terminals)

$$I_{io} = |I_{B_1} - I_{B_2}|$$

3. Input bias current :
   It is the average of the currents that flow into inverting and non-inverting input terminals of an op-amp.

$$I_{ib} = \frac{I_{B1} + I_{B2}}{2}$$

4. Gain
   Differential mode gain A_d is the gain of op-amp when two different voltages are applied at two inputs.
   Common mode gain A_{cm} is the gain of op-amp when two terminals of op-amp are supplied with same voltage from same source.

5. CMRR [Common mode Rejection Ratio]:
   CMRR is defined as the ratio of differential voltage gain A_d to common mode gain A_{cm}

$$CMRR = \left| \frac{A_d}{A_{cm}} \right|$$

6. Slew Rate:

It is the maximum rate of change of o/p voltage per unit time and is expressed in Volts per microseconds.

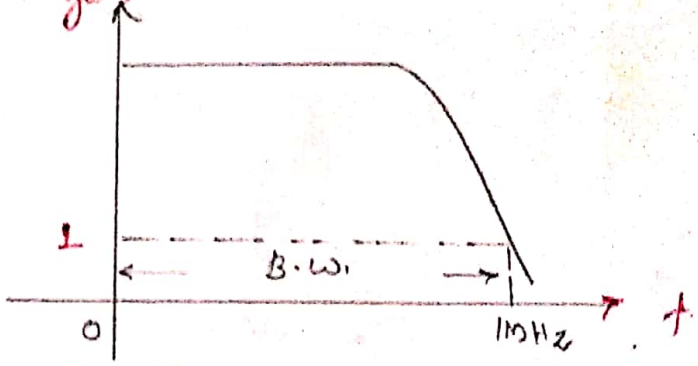
$$SR = \left.\frac{dV_o}{dt}\right|_{max} \text{ V/µs.}$$

Slew rate indicates how fast the o/p of an op-amp can change in response to changes in input frequency.

$$SR = 2\pi f V_m \times 10^{-6} \text{ V/µs.}$$

7. Unity Gain - Bandwidth product

It is the bandwidth of an op-amp when the voltage gain is unity.

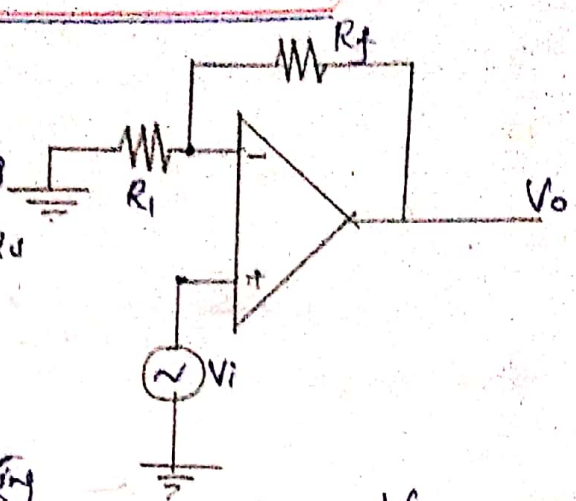


Comparison of IDEAL & PRACTICAL Op-amps

Characteristics	Ideal	Practical (741)
Input impedance, R_i	∞; Infinity	~~2MΩ~~
O/p impedance, R_o	0	~~75Ω~~
Voltage gain, A_V	∞; infinity	200,000
Band width	infinity	1MHz ~~2MHz~~
Slew Rate	infinite	0.5 V/µs
CMRR	infinite	90 dB.
offset voltage	zero.	~~2mV~~ 2mV to 6mV.

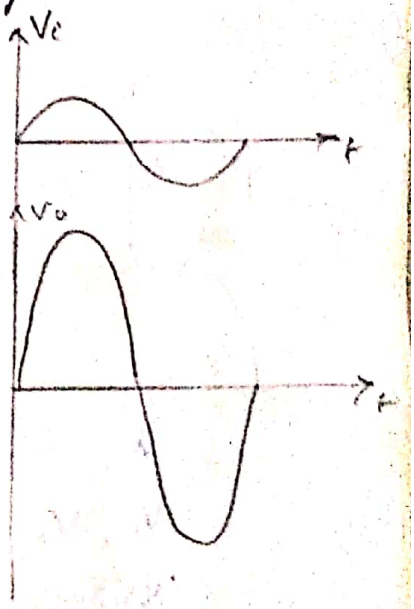
Applications of Op-amp

Non Inverting Amplifier / Scale Changer



In Non inverting amplifier o/p is given to Non-inverting terminal and thus-fro o/p is in phase with input

Due to virtual ground voltage at non inverting terminal will be equal to supply voltage Vi

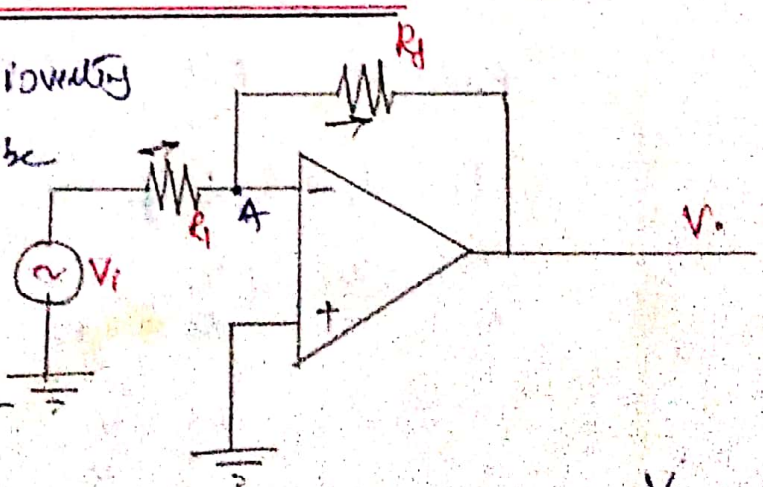


Now $V_i = V_o \times \frac{R_1}{R_1 + R_f}$

$$\text{Gain} = \frac{V_o}{V_i} = \frac{R_1 + R_f}{R_1}$$

$$A_v = 1 + \frac{R_f}{R_1}$$

Inverting Amplifier / Sign Changer



Here o/p is given to inverting terminal ∴ o/p will be 180° out of phase with input.

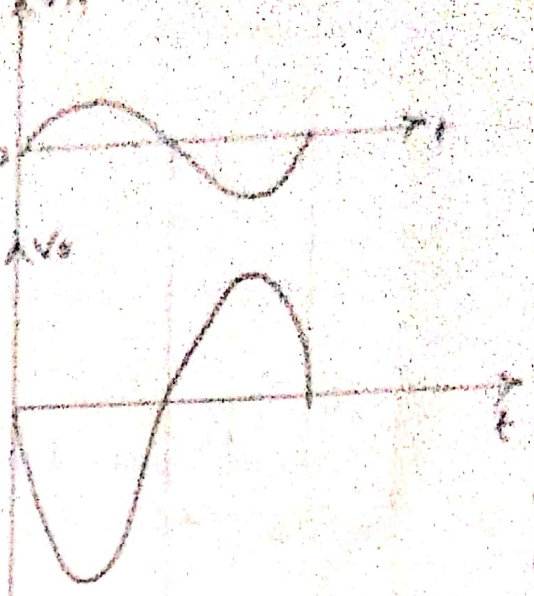
By applying Node at Point A ; $V_A = 0$.

$$\frac{V_A - V_i}{R_1} + \frac{V_A - V_o}{R_f} = 0.$$

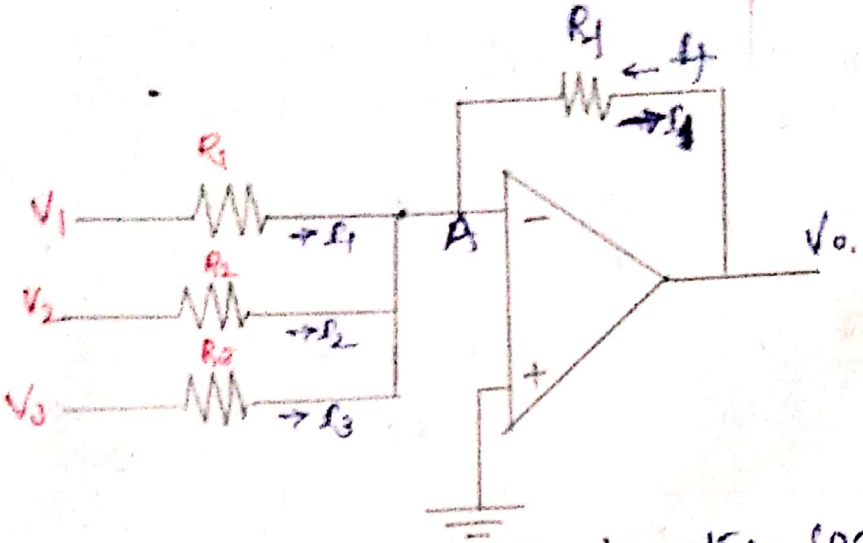
$$\therefore \frac{-V_i}{R_1} - \frac{V_o}{R_f} = 0.$$

$$\frac{V_o}{R_f} = \frac{-V_i}{R_i}$$

$$A_V = \frac{V_o}{V_i} = \frac{-R_f}{R_i}$$



Summing Amplifier / Adder



It is also used in inverting configuration. Here V_1, V_2 and V_3 are connected to inverting input terminal through resistors R_1, R_2 & R_3 resp. O/p voltage will be the sum of input voltages.

Applying KCL at node A

$$I_f = -I$$

$$I_1 + I_2 + I_3 = I_f$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_o}{R_f}$$

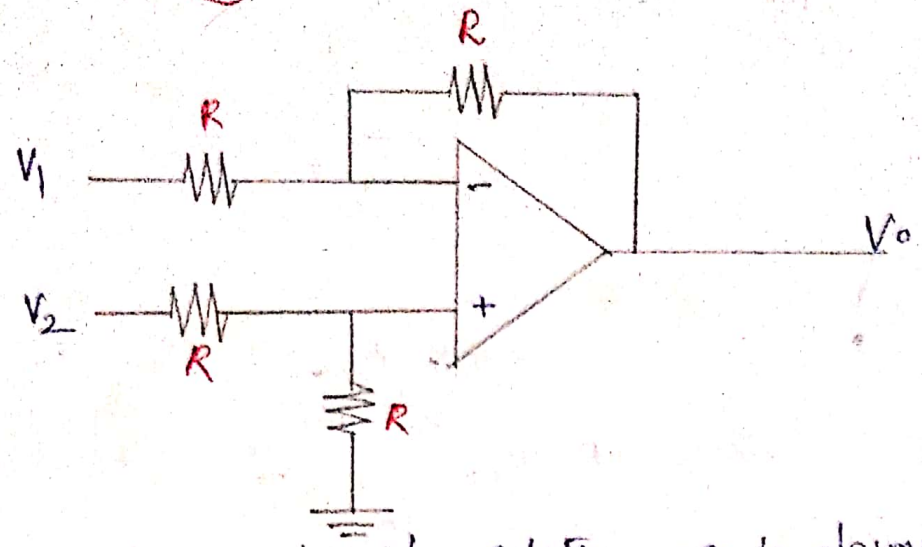
$$V_o = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

If $R_1 = R_2 = R_3 = R_f = R$ then

$$V_o = -[V_1 + V_2 + V_3]$$

Subtractor or Difference Amplifier

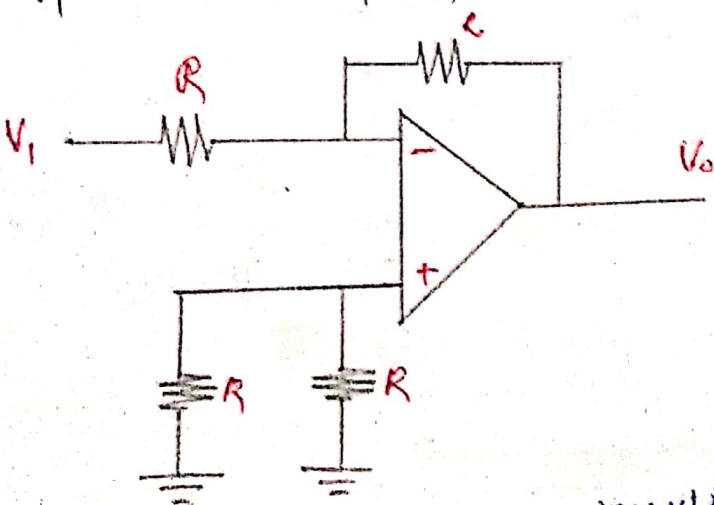
The subtraction of two input voltages is possible with the help of Op-amp ckt called Subtractor or Difference amplifier circuit.



The inputs and o/p relation can be found by using Super position principle

Let V_1 is the only input ; $V_2 = 0$; and o/p is V_{o1}

Then

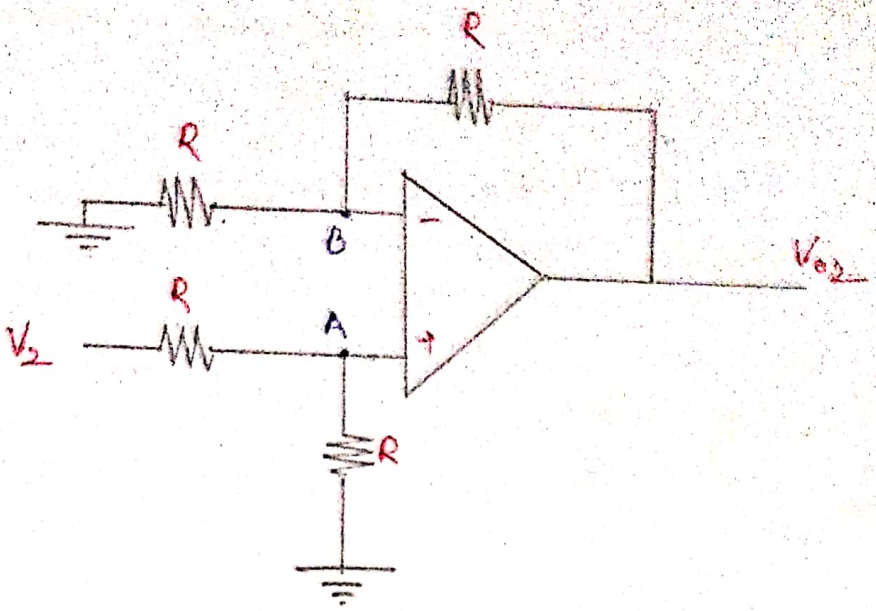


Now the ckt act as an inverting amplifier and

Thus o/p $V_{o1} = V_1 \times \frac{-R}{R}$

$$V_{o1} = -V_1 \quad \text{---} \quad (1)$$

Now only V_2 as input & $V_1 = 0$; o/p is V_{o2}



Now Voltage at point A ; $= V_2 \times \frac{R}{2R} = \frac{V_2}{2}$

Voltage at point B is equal to V_2 by Virtual ground property

$\therefore \quad V_B = V_2$

Now $\quad V_{o2} \times \frac{R}{2R} = V_2$

$\Rightarrow \quad V_{o2} = V_2 \quad \ldots\ldots (2)$

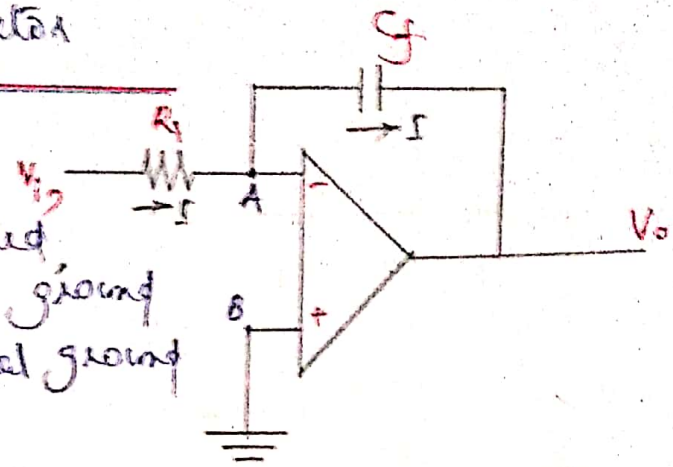
The total o/p voltage V_o can be found by adding eqn (1) & (2)

$\Rightarrow \quad \boxed{V_o = V_2 - V_1}$

Integrator:

In an integrating circuit, o/p voltage is the integration of input voltage. The integrator ckt without using op-amp or transistors etc is called passive integrator. While an integrator using active devices like Op-amp is called active integrator.

Active Op-amp Integrator



Here node B grounded
node A is also at ground potential due to virtual ground

$\therefore \quad V_B = V_A = 0.$

As input current to Op-amp is zero, the entire current I flows through R_1 & C_f.

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1}$$

Current through capacitor

$$I = C_f \frac{d(V_A - V_o)}{dt}$$

$$= -C_f \frac{dV_o}{dt}$$

Since both currents are equal

$$\frac{V_{in}}{R_1} = -C_f \frac{dV_o}{dt}$$

$$\frac{dV_o}{dt} = \frac{-1}{R_1 C_f} \cdot V_{in}$$

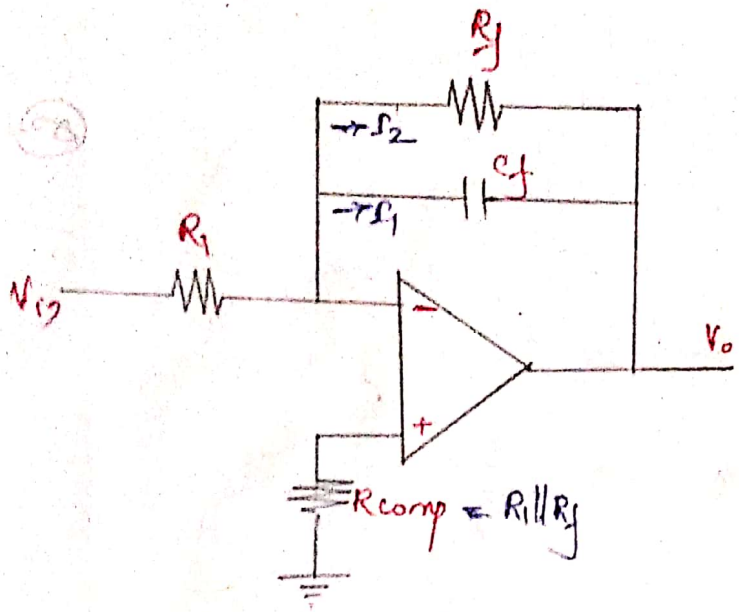
$$\boxed{V_o = \frac{-1}{R_1 C_f} \int V_{in}\, dt} \quad \& \quad V_o \propto \int V_{in}$$

Limitations of Ideal Integrator

The Operational amplifier has input offset voltage V_{IOS} and input bias current I_B. These two components can produce an error voltage at o/p and may cause the Op-amp to saturate. It is very difficult to pull the Op-amp out of saturation.

Another limitation of ideal integrator is its low bandwidth. Hence it can be used for only for small frequency range of input only.

Practical Integrator:



The limitations of ideal Op-amp integrator can be minimized in practical integrator ckt.

The resistance R_{comp} is used to overcome errors due to bias current.

R_f reduces low frequency gain of Op-amp.

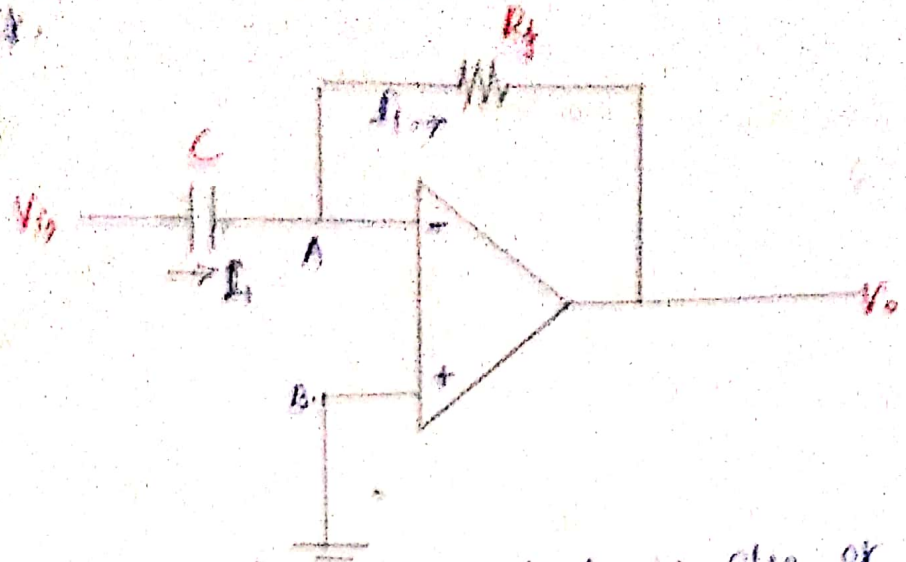
Applications of Integrator:

1. In analog computers.
2. In solving differential equations.
3. In analog to digital converters.
4. In ramp generators.
5. In various wave shaping circuits.

DIFFERENTIATOR:

In a differentiator o/p will be proportional to differential of i/p.

i/p.



Here node B Grounded hence A is also at Ground potential. The input current to op-amp is zero entire current I_1 flows through R_f.

From input side $I_1 = C \frac{d(V_{in} - V_A)}{dt} = C \frac{dV_{in}}{dt}$

From o/p side $I_1 = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f}$

equating both equations

$$C \frac{dV_{in}}{dt} = \frac{-V_o}{R_f}$$

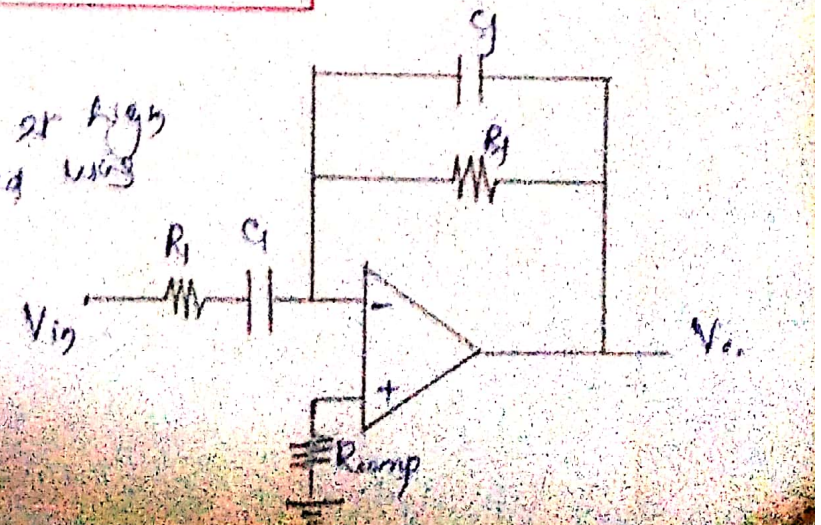
$$\boxed{V_o = -C_1 R_f \cdot \frac{dV_{in}}{dt}}$$

$V_o \propto \frac{dV_{in}}{dt}$

Practical Differentiator:

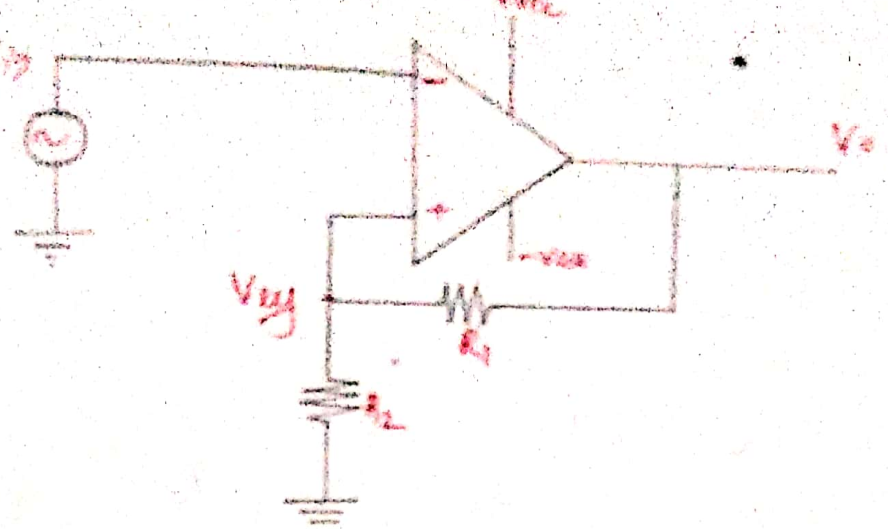
The Noise and Instability at high frequency can be corrected using practical Differentiator.

Ramp is used for bias compensation



Schmitt Trigger [Regenerative Comparator]

Schmitt trigger is a Sine wave to Square wave converter, which uses a +ve feedback. It is also called Regenerative Comparator.



Here the input is applied to the inverting terminal. The inverting mode produces opposite polarity output. The feedback to non-inverting input ensures positive feedback.

When V_{in} is slightly +ve than V_{ref}, o/p gets driven into negative saturation i.e. at $-V_{sat}$ level.

When V_{in} becomes more −ve than $-V_{ref}$, then o/p gets driven into positive saturation. Thus o/p voltage is always at $+V_{sat}$ or $-V_{sat}$. But the voltage at which it changes its state can be controlled by R_1 & R_2.

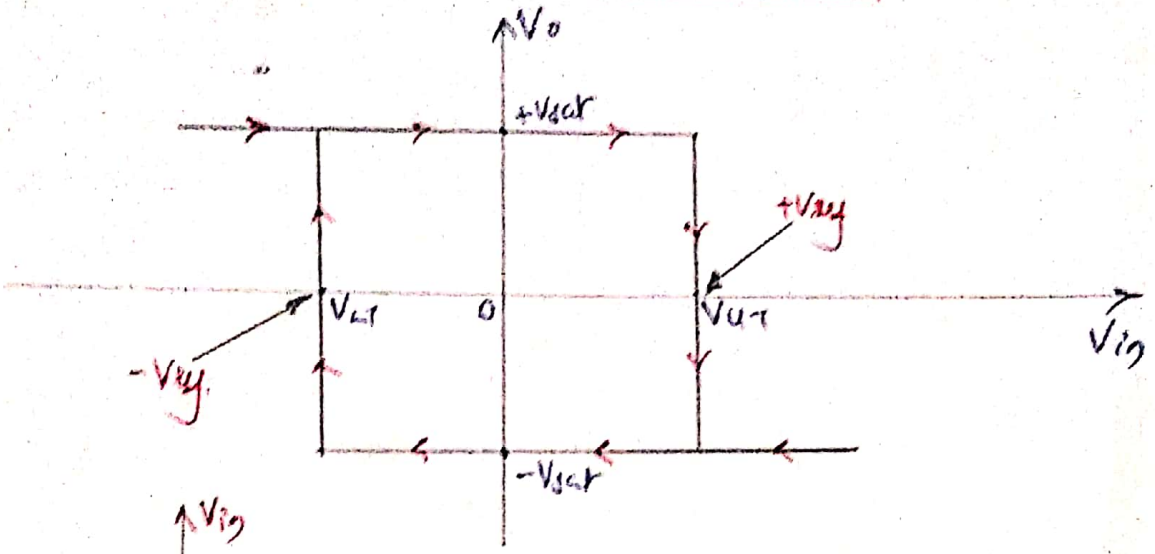
From voltage divider $+V_{ref} = V_o \times \frac{R_2}{R_1+R_2} = \frac{+V_{sat} \cdot R_2}{R_1+R_2}$

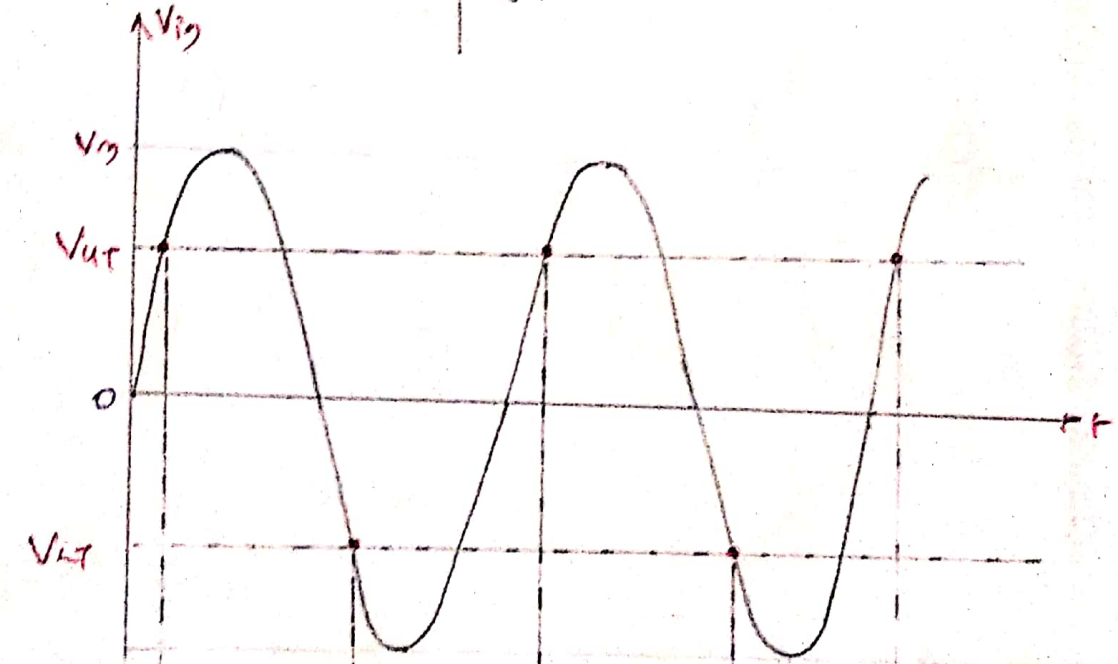
$$-V_{ref} = \frac{-V_o \times R_2}{R_1+R_2} = \frac{-V_{sat} \times R_2}{R_1+R_2}$$

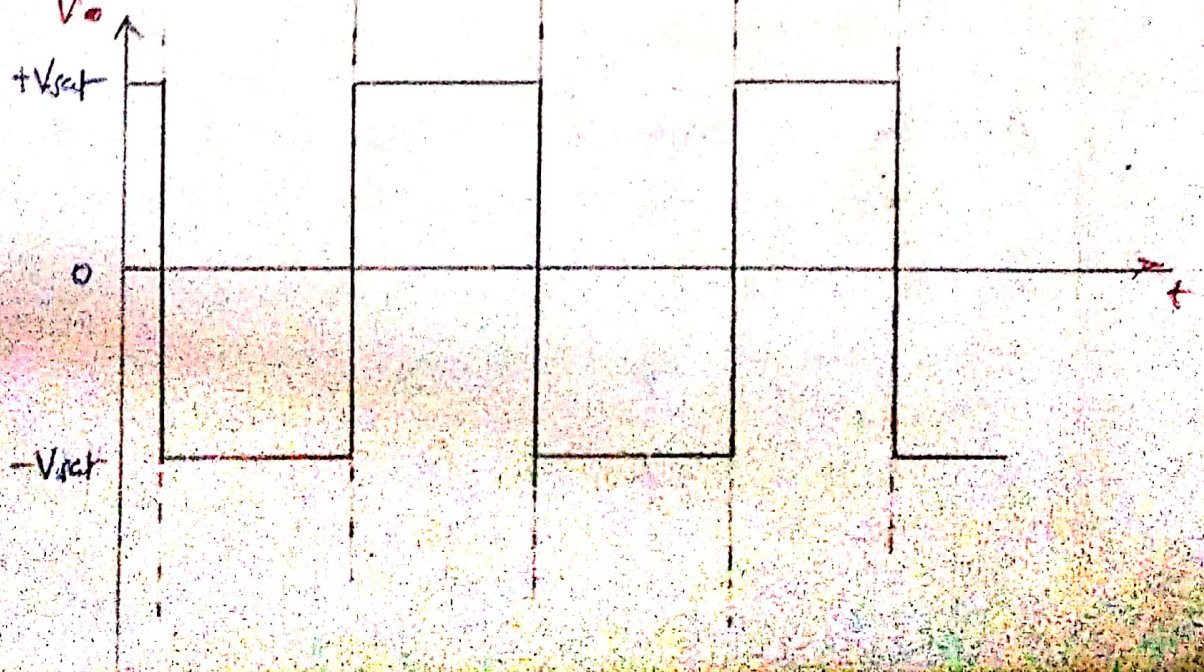
$+V_{ref}$ is called Upper Threshold voltage denoted by V_{UT} and $-V_{ref}$ is called Lower Threshold voltage denoted by V_{LT}

$$V_{UT} = +V_{sat} \times \frac{R_2}{R_1 + R_2}$$

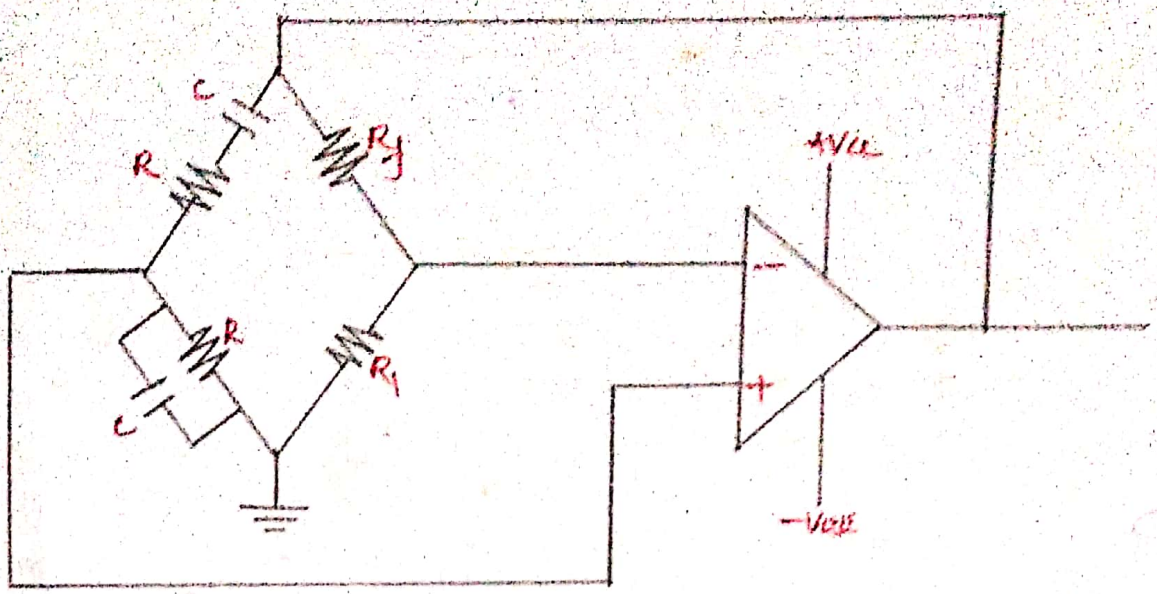
$$V_{LT} = -V_{sat} \times \frac{R_2}{R_1 + R_2}$$

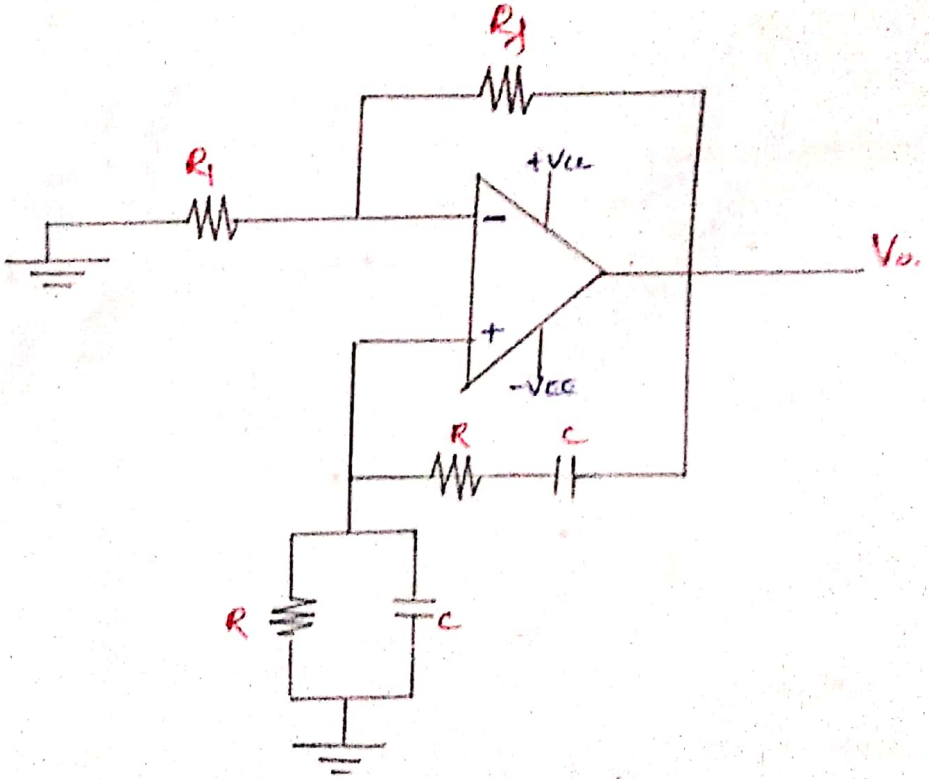






WIEN BRIDGE OSCILLATOR:





Here the resistance R & capacitor C are the components of frequency sensitive arms of the bridge. The resistance R and Rf are the pair of feedback path.

The gain of the op-amp is

$$A = 1 + \frac{R_f}{R_1}$$

To satisfy Barkhausen criterion $A\beta \geq 1$, it is necessary that the gain of non-inverting amplifier must be minimum 3

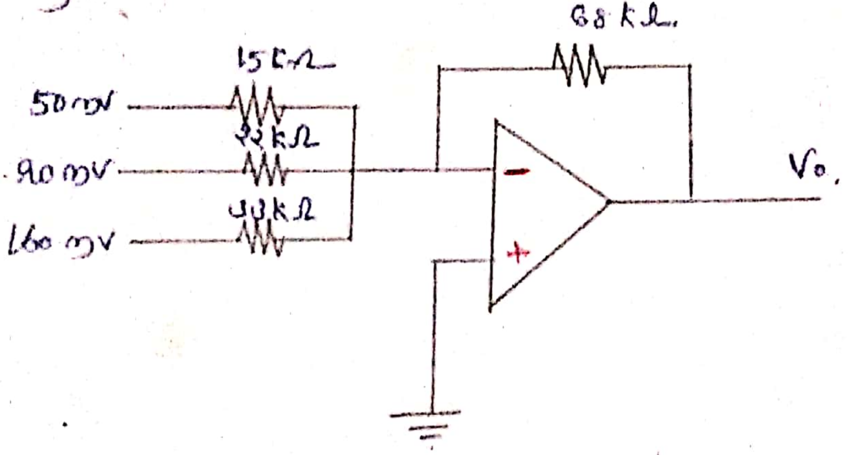
$$|A| \geq 3 \quad \text{i.e.} \quad 1 + \frac{R_f}{R_1} \geq 3$$

$$\boxed{\frac{R_f}{R_1} \geq 2}$$

The frequency of oscillation is given by

$$\boxed{f = \frac{1}{2\pi RC} \text{ Hz}}$$

Prob: ① In figure; what is the o/p voltage ?



$$V_o = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

$$= -68k \left[\frac{50m}{15k} + \frac{90m}{22k} + \frac{160m}{33k}\right]$$

$$= -834.5 \text{ mV}$$

② Design an NI amplifier with gain 10.

③ Design an inverting amplifier with gain 20.

④ Design an integrator with cut off freq 2kHz.

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Scheme -1
Number of

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MODULE 6

MODULE VI
INTEGRATED CIRCUITS.

: ACTIVE FILTERS :

A filter is a circuit that is designed to pass specified band of frequencies while attenuating all the signals outside that band.

Filters are basically classified as active and passive filters.

Passive filter networks use only passive elements such as resistors, inductors and capacitors.

Active filter circuits use active elements such as op-amps, transistors along with resistors and capacitors.

: Advantages of Active filters :

1. All the elements along with op-amp can be used in the integrated form. Hence there is reduction in size and weight.
2. In large quantities, the cost of IC can be much lower than its equivalent passive network.
3. Op-amp has high input impedance and low o/p impedance hence active filters using op-amp do not cause loading of source or load.
4. The inductors are absent in active filters. Hence they are more economical.
5. The design procedure is simple than passive filters.
6. Active filters can provide voltage gain, whereas the passive filters often show a significant voltage loss.

Limitations of Active filters:

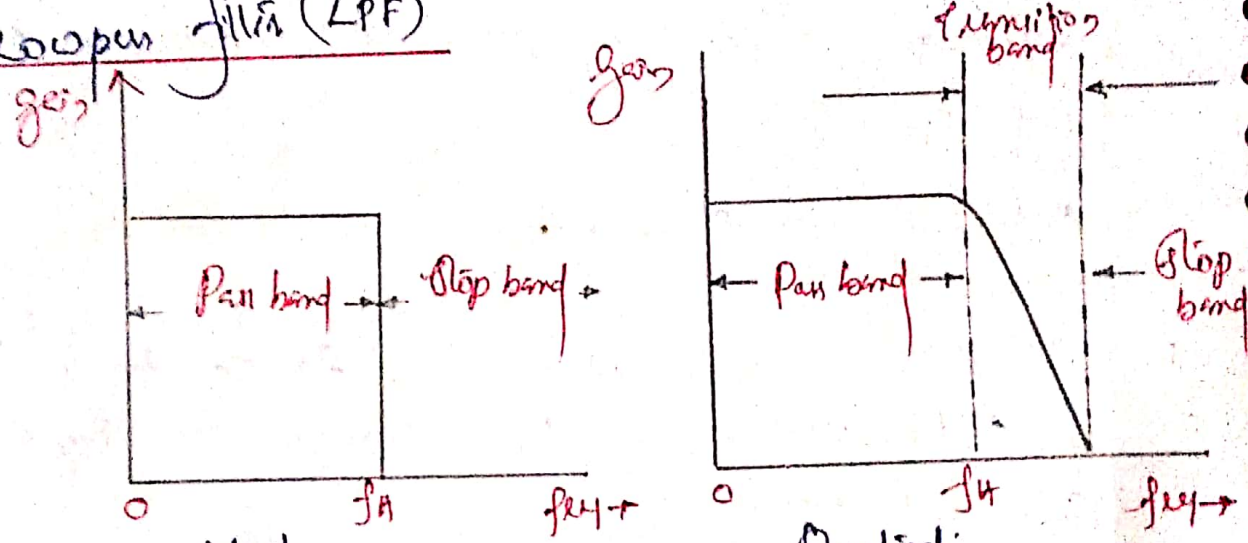
1. Fixed Bandwidth.
2. Sensitive to temperature and environmental changes.
3. Requirement of dc power supply.

Most Commonly used filters are

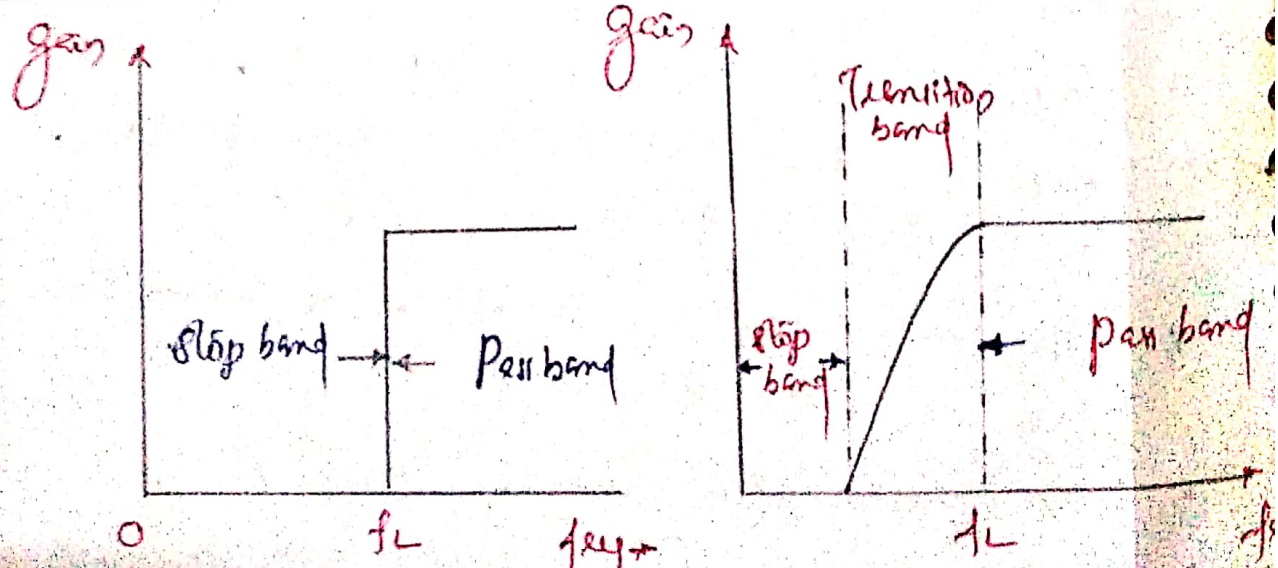
* Low pass RC filter * High pass filter * Band pass filter
* Band Reject / Band Stop filter * All pass filter.

Frequency Response Characteristics of filters:

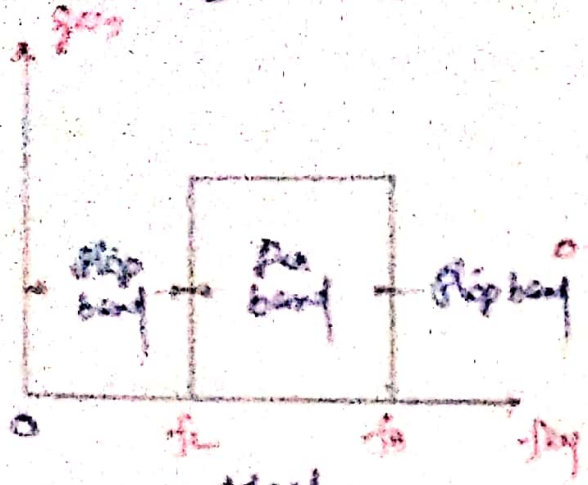
1 Low pass filter (LPF)



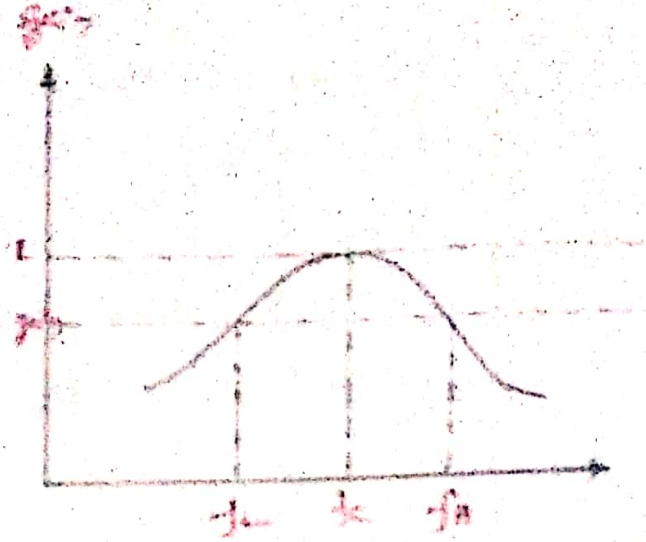
2 High pass filter (HPF)



Band Pass filter (BPF)

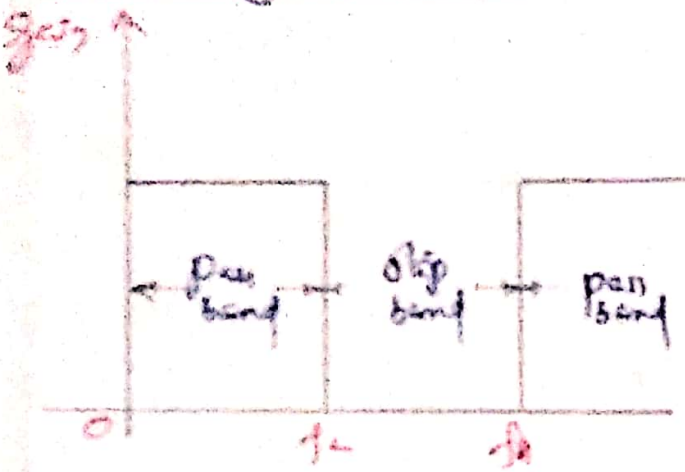


ideal

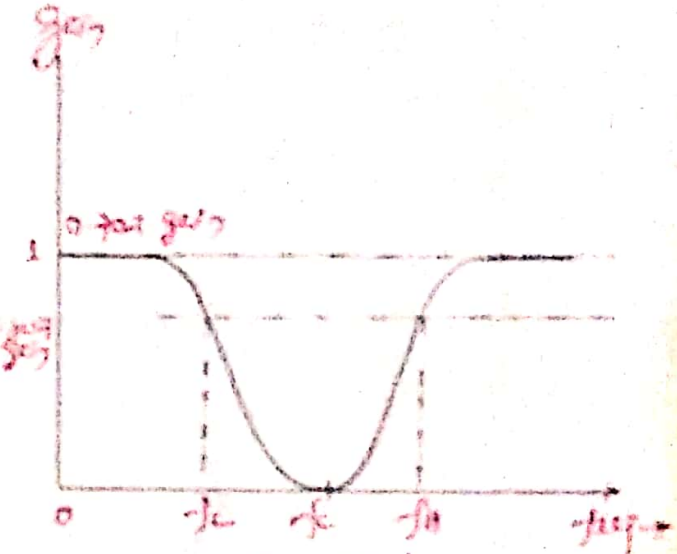


Practical

Band Reject filter (BRF)

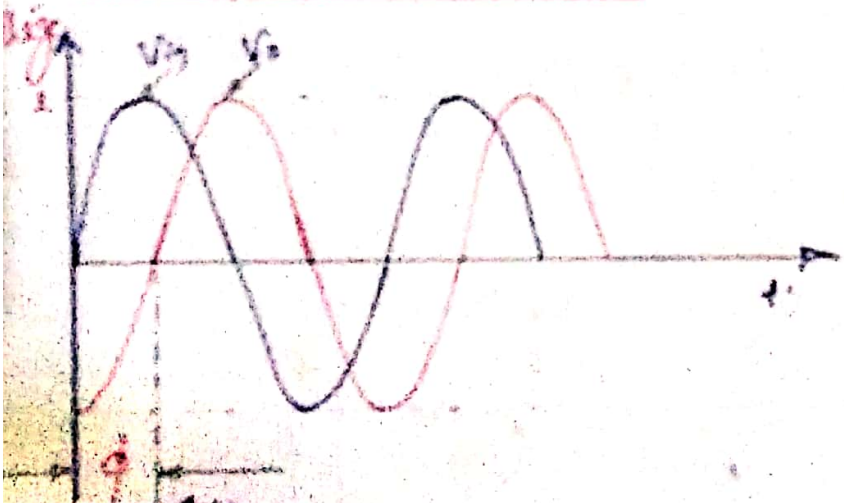


ideal



Practical

All pass filter:



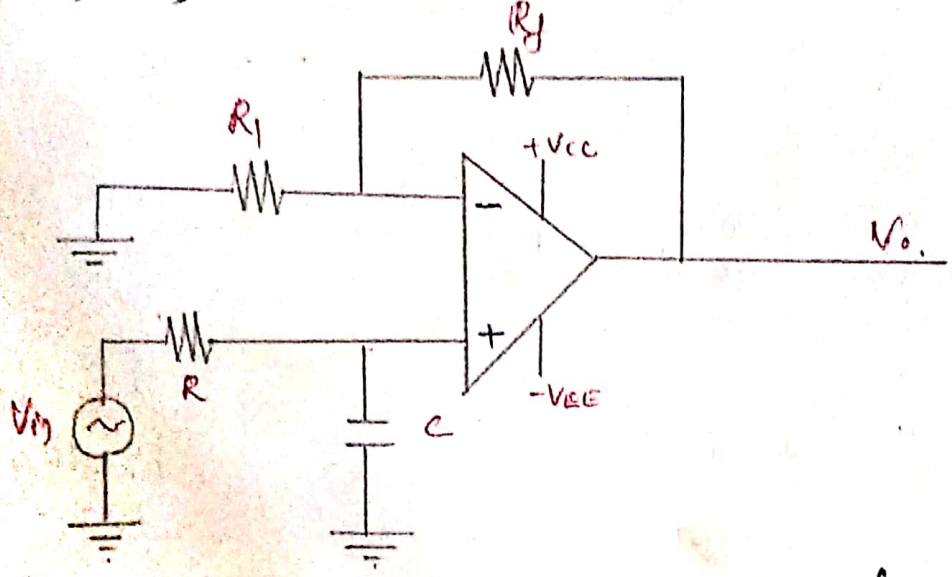
phase shift

All pass filter passes all frequencies but it produces the phase shift between input and output.

the rate at which gain of filter changes in the stop band, depend on Order of filter. For a first order filter (with one capacitor) gain increases at a rate of 20 dB/decade in stop band of diff. If it is 2nd order filter (with 2 capacitors) gain increase will be at 40 dB/decade.

First Order Low pass Butterworth filter.

Butterworth filter has a flat pass band flat stop band. ∴ it is also called maximally flat or flat-flat filter.



First order filter with RC Network for filtering is shown in figure. Op-amp is used in non-inverting configuration. Gain of filter is determined by resistors R_1 & R_f.

$$\text{Gain of filter} = \frac{V_{out}}{V_{in}} = \frac{A_f}{1+j\frac{f}{f_H}}$$

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{A_f}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}$$

$$A_f = 1 + \frac{R_f}{R_1}$$

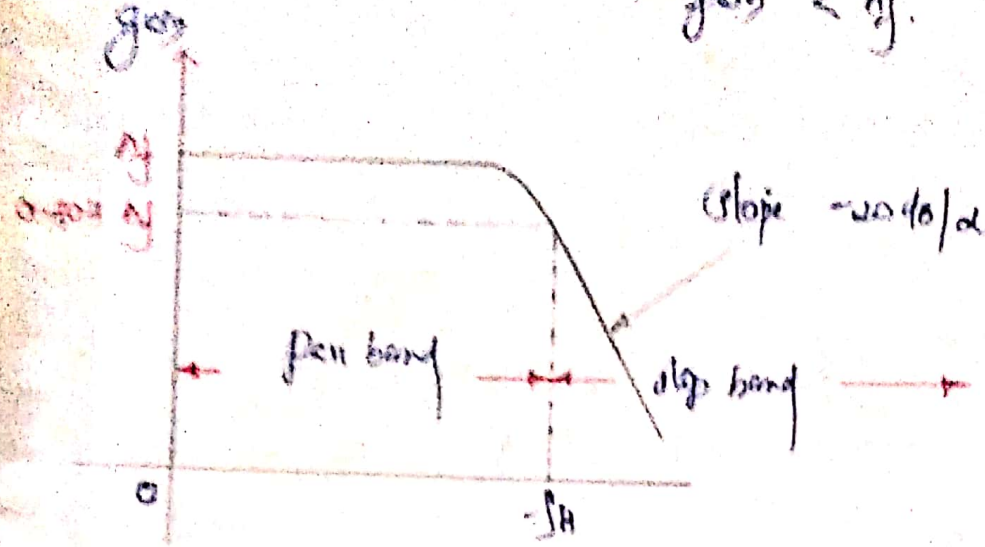
For low freq. $f < f_H$ gain = A_f.

For freq equal to f_H ; $f = f_H$

gain = $\frac{A_f}{\sqrt{2}}$ or $0.707 A_f$.

For freq greater than f_H : $f > f_H$

gain < A_f.

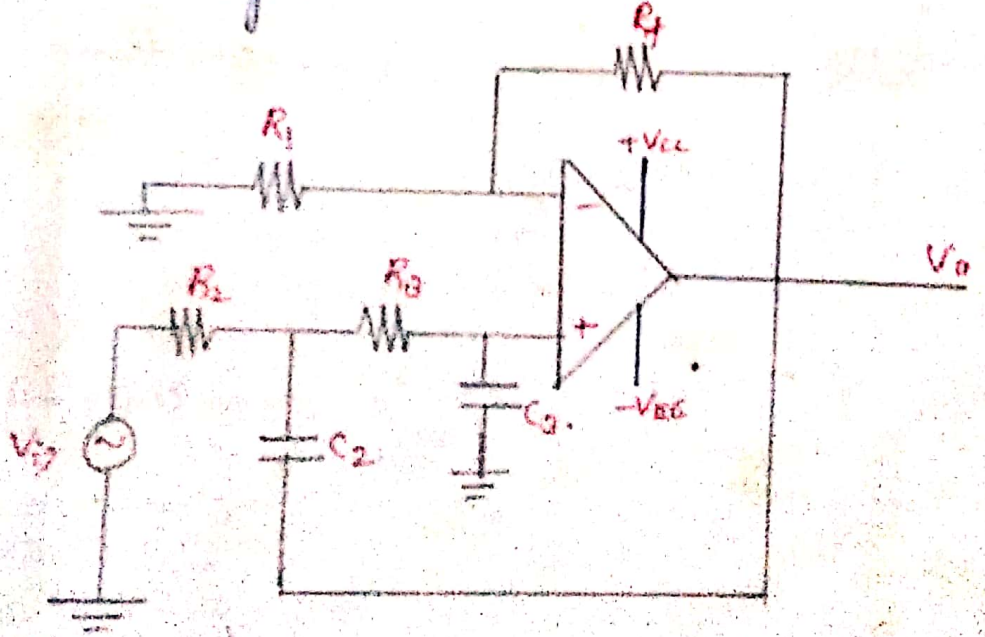


$$f_H = \frac{1}{2\pi RC}$$

Second Order Low pass Butterworth filter

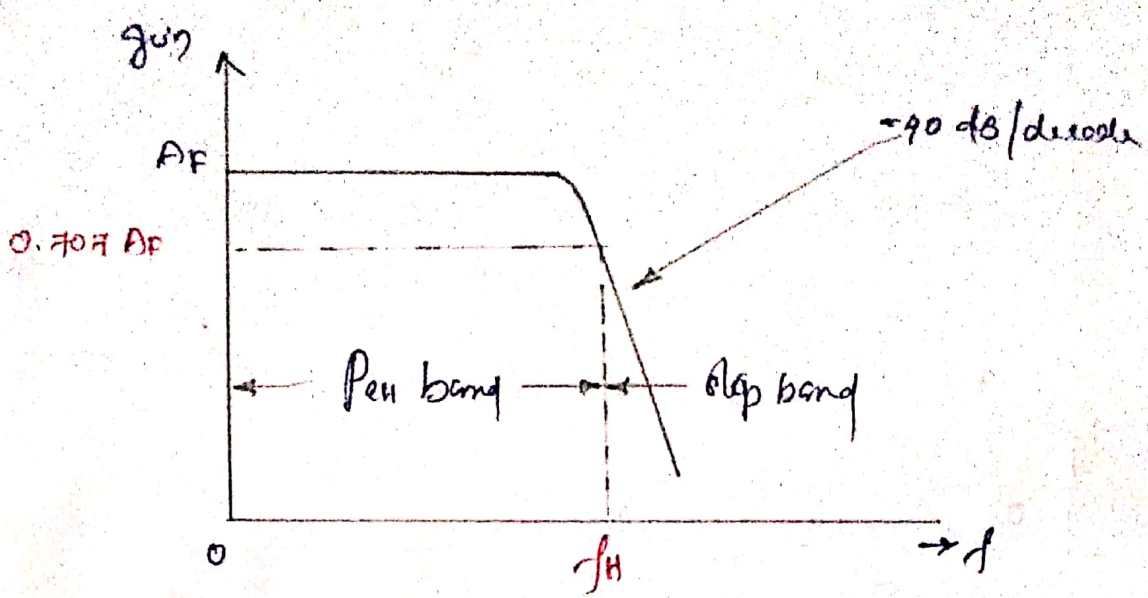
Frequency response of practical filter must be very close to ideal one. For fast gain roll off we can use higher order filters.

A 2nd order Butterworth filter has gain roll off of 40db/dec. It uses two capacitors and two resistors at input side which decide cut off frequency



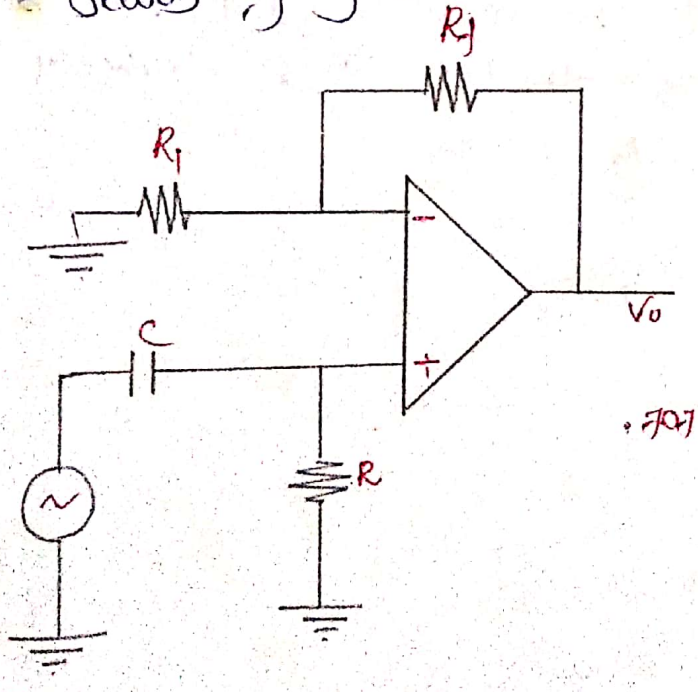
$$\text{gain} = \frac{A_F}{\sqrt{1+(f/f_H)^2}} \qquad A_F = 1 + \frac{R_f}{R_1}$$

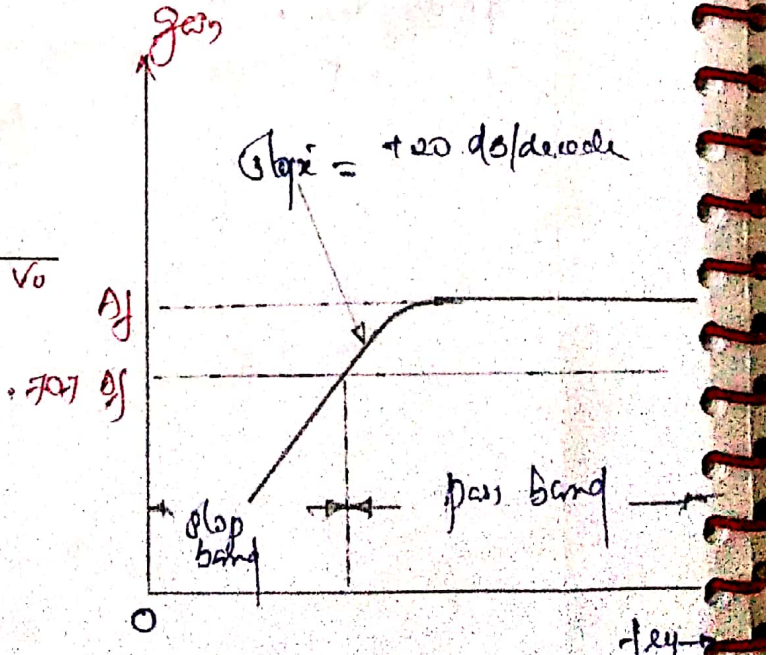
$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} = \frac{1}{2\pi RC}$$



First Order HP Butterworth filter:

High pass active filter is the complement of low pass active filter and is formed simply by exchanging the place of resistors and capacitors in the frequency determining section of filter.





This ckt passes high frequencies but blocks low frequencies. cut off freq is given by $\frac{1}{2\pi RC}$.

Below this freq (fL) o/p voltage decreases at a rate of 20dB/decade.

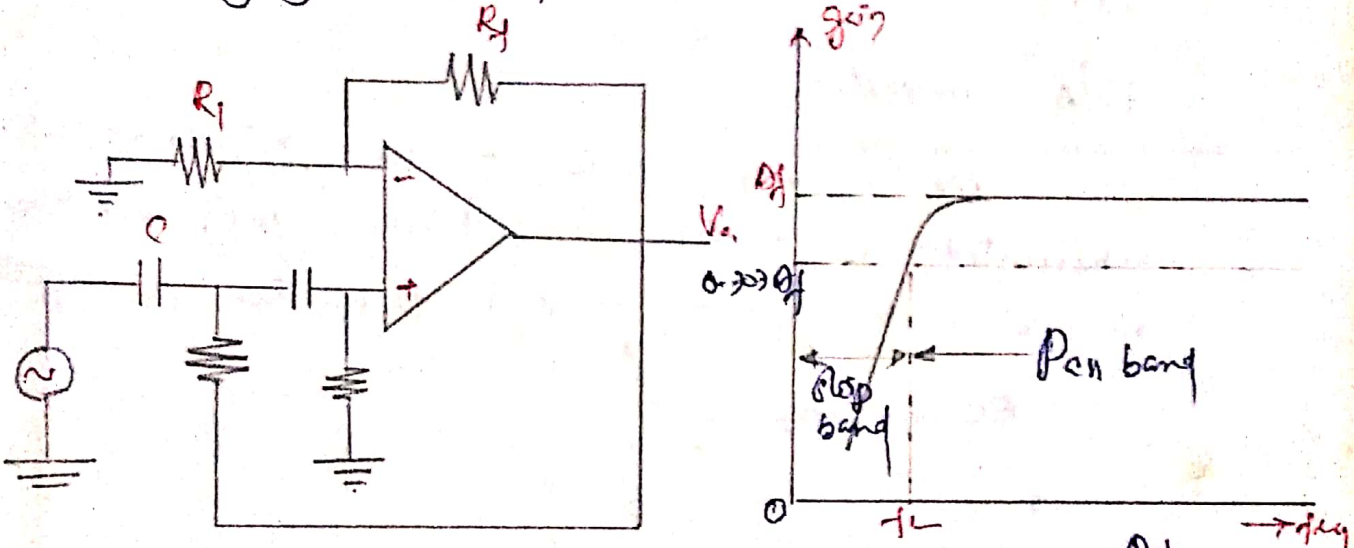
$$\frac{V_o}{V_{in}} = \frac{A_f}{\sqrt{1+(f_L/f)^2}}$$

Gain $A_F = 1 + \frac{R_f}{R_1}$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}}$$

2nd Order HP Butterworth filter

A 2nd order HP Butterworth filter can be formed from 2nd order LP Butterworth filter simply by interchanging frequency determining resistors and capacitors.



Voltage gain of 2nd order HPF is $\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}}$

$A_f = 1 + \frac{R_F}{R_1}$

Gain roll of of 2nd order HPF will be 40dB/dec.

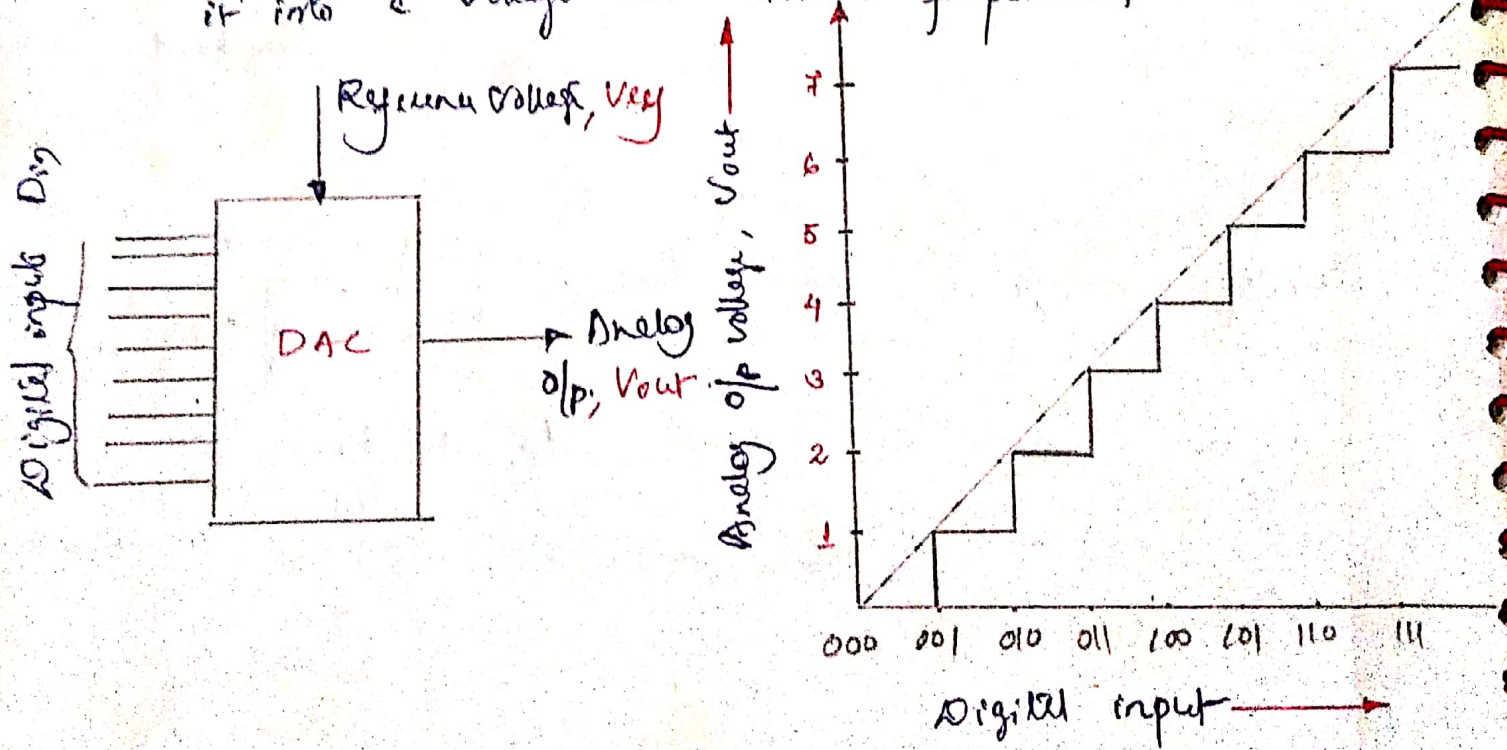
Analog to Digital & Digital to Analog Converters:

Most of information carrying signals are available in the analog form (voltage, current, temperature, pressure). But digital systems (such as microprocessor) use binary system of ones & zeros (Digital), we have to convert signal from analog form to digital form. The circuit that performs this conversion is called Analog to Digital converter (A/D converter).

Digital to analog converter is used when a binary output from a digital system is to be converted to some convenient analog voltage or current.

: D/A converter:

D/A conversion is the process of taking a value represented in digital code (binary or BCD) and converting it into a voltage or current proportional to digital value.



Specifications of DAC.

* Resolution:

Resolution is defined as the range of the smallest change that can occur in an analog output as a result of a change in digital input.

$$\% \text{ resolution} = \frac{\text{Step size}}{\text{Full scale}} \times 100.\ \%$$

Full scale = number of steps × step size.

$$\% \text{ Resolution} = \frac{1}{\text{Total Number of Steps}} \times 100\ \%$$

for N bit DAC number of steps will be $2^N - 1$

* Accuracy:

It is a comparison of actual o/p voltage with expected o/p. It is expressed in percentage.

Accuracy can specify in terms of Full scale error or linearity error.

Full scale error is the maximum deviation of DAC's o/p from its expected value, expressed as the percentage of full scale.

Linearity error is the maximum deviation in step size from ideal step size.

* Monotonicity

A converter is said to have good monotonicity if it does not miss any step when stepped through entire range by a counter.

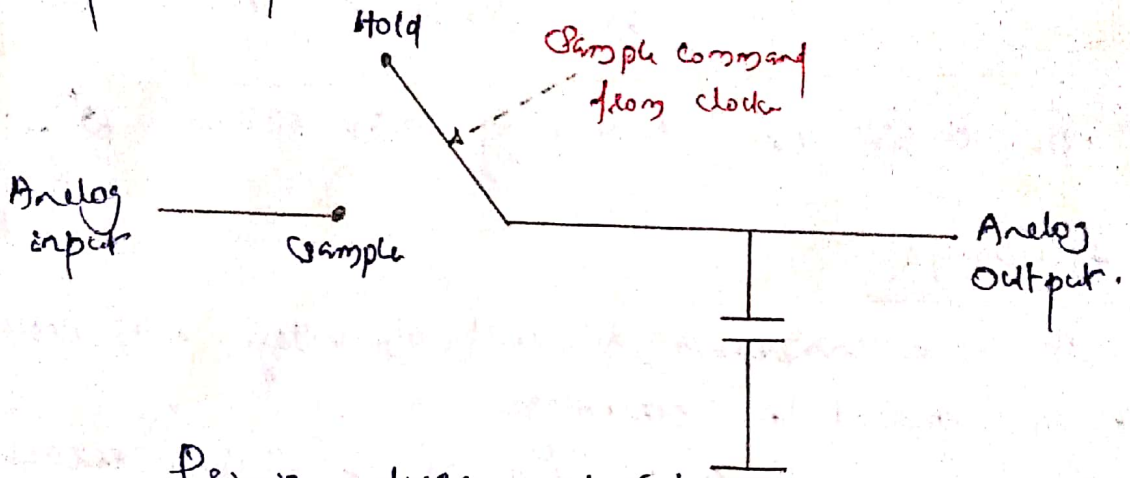
* Conversion time:

It is the time required for conversion of digital signal into analog equivalent. It is also called settling time.

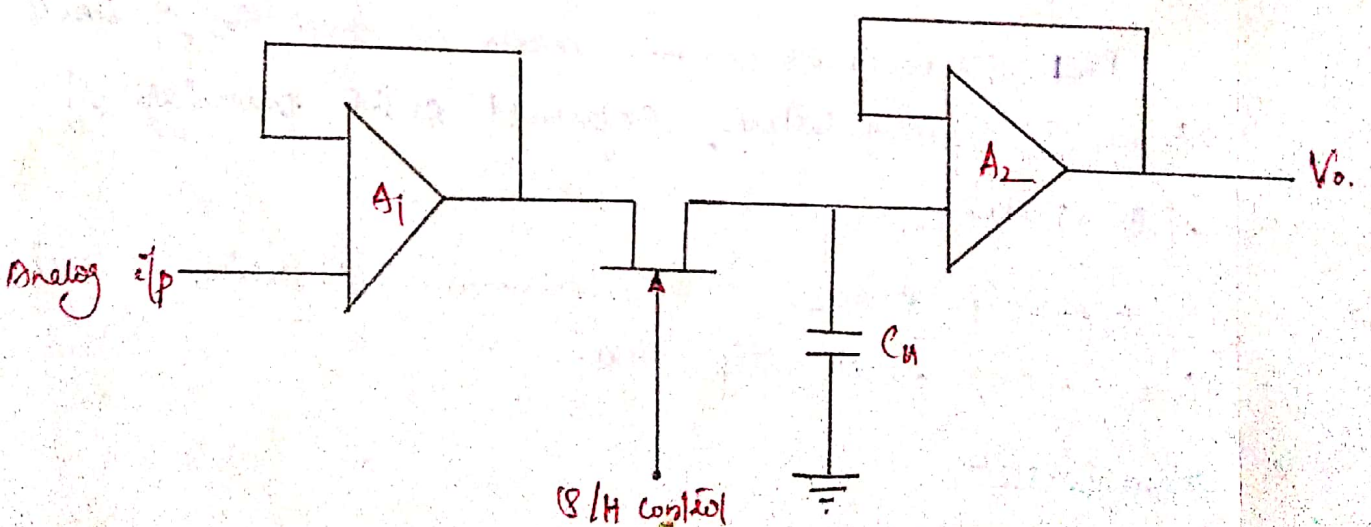
Sample and Hold circuit: (S/H ckt)

Sample and hold circuit samples the value of input signal in response to a sampling command and hold it at the o/p until the arrival of next command.

S/H circuit uses two basic components analog switches and a capacitor.

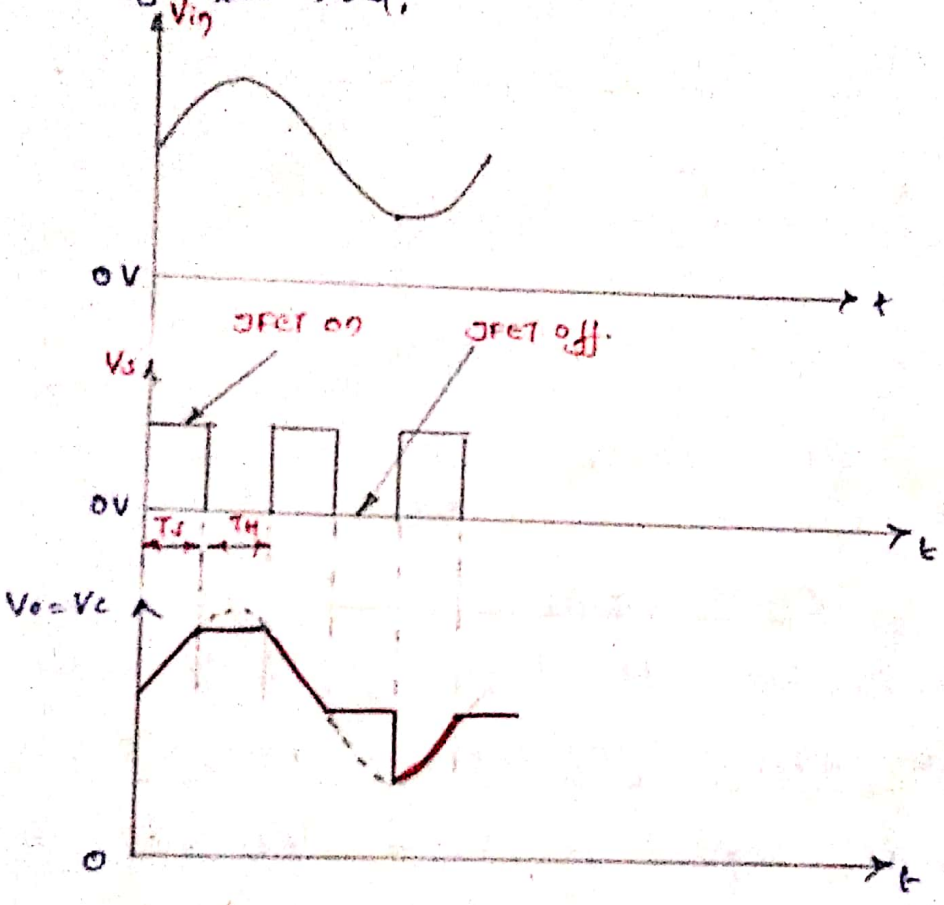


Principle diagram of S/H ckt.



Basic Sample and hold ckt is shown in figure. Here JFET is used as switch. During sampling time, JFET switch is ON, and holding capacitor charges up to the

level of the analog o/p voltage at the end of sampling period, JFET turned off. This isolates the holding capacitor C_H from input signal. Hence the o/p voltage will remain constant at the value of input voltage at the end of sampling time. But there will be some voltage drop at capacitor because of various leakage currents. To avoid this, input and output buffers (voltage follower) circuits are used.



R - 2R Ladder Type DAC

It uses a ladder network containing series and parallel combinations of two resistors of values R & 2R. Hence the name. The Operational amplifier configured as voltage follower is used to prevent loading.

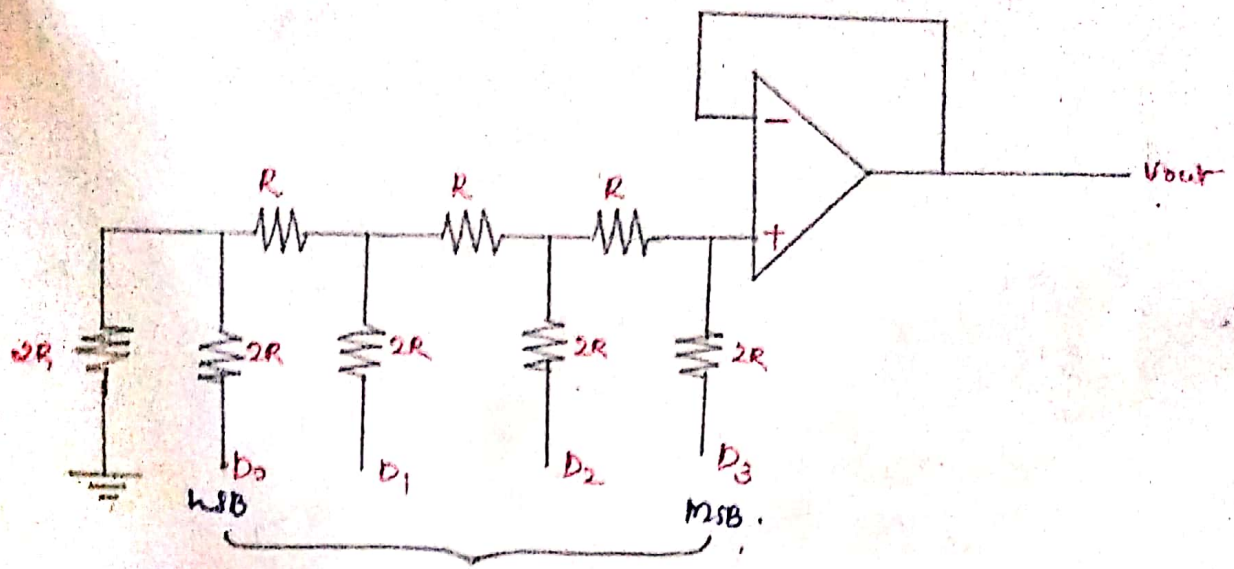


Figure shows the ckt diagram of R-2R ladder type DAC. It has 4 bit digital input. When digital signal $D_3D_2D_1D_0$ is applied at input terminals, analog signal is produced at o/p terminal.

When D_0 input is 1 and all other inputs are zero then the o/p level caused by the D_0 bit

$$V_{out} = \frac{E}{2^{N-1}}$$

N is the total Number of Binary inputs.

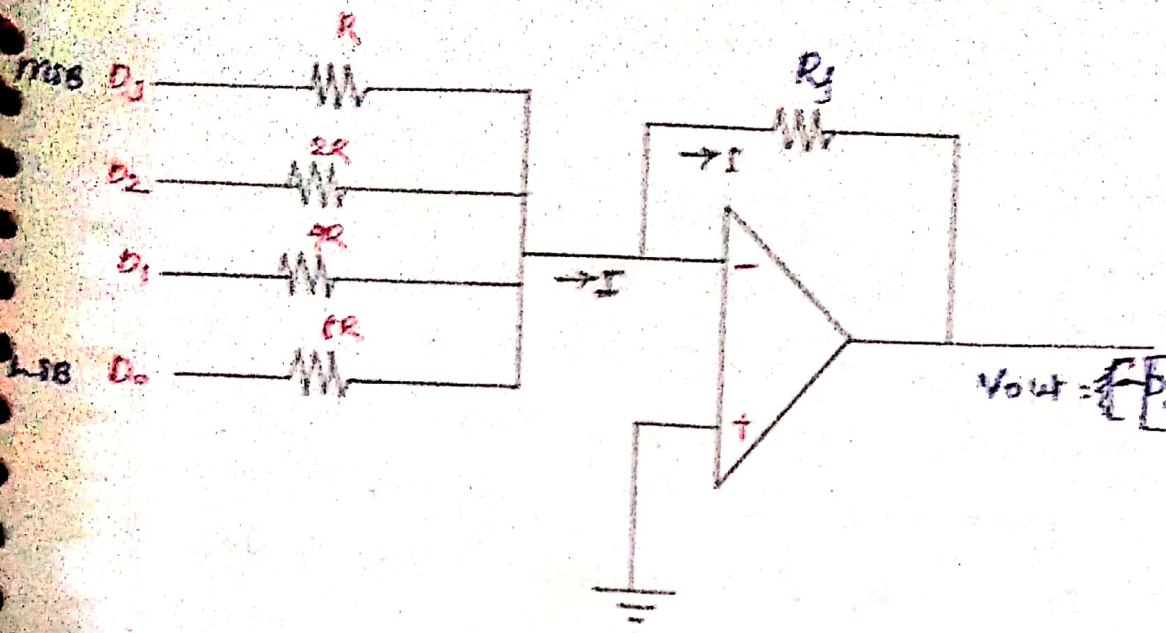
Example: If E = 5V then o/p voltage when input is 0100 is.

$$V_{out} = \frac{5}{2^{4-2}} = \frac{5}{4} = 1.25V$$

When more than 1 input is high

$$V_0 = -V_R\left(b_1 2^{-1} + b_2 \cdot 2^{-2} + b_3 \times 2^{-3} + \dots + b_n \cdot 2^{-n}\right)$$

The Weighted Resistor type DAC



Here the Op amp is used to produce a weighted sum of digital inputs, where the weights are proportional to the weights of bit positions of inputs. Since Op-amp is connected as an inverting amplifier, each input is amplified by a factor equal to the ratio of R_f divided by input resistance to which it is connected. The MSB D_3 is amplified by $\frac{R_f}{R}$, D_2 is amplified by $\frac{R_f}{2R}$, D_1 is amplified by $R_f/4R$ & D_0 is amplified by $R_f/8R$.

The inverting terminal of Op-amp act as Virtual ground. Since the Op-amp adds and inverts

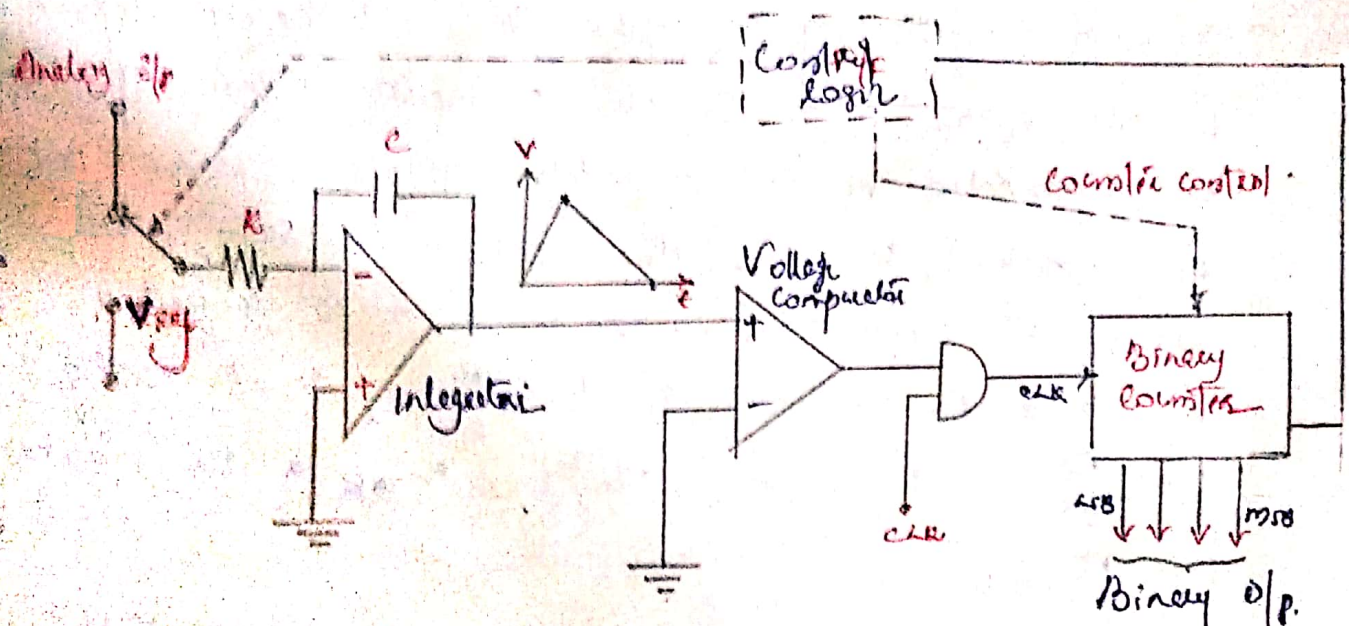
$$V_{out} = -\left[D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8}\right] * \frac{R_f}{R}$$

Analog to Digital Conversion

ADC produces digital output that is proportional to the value of input analog signal.

Dual slope type ADC

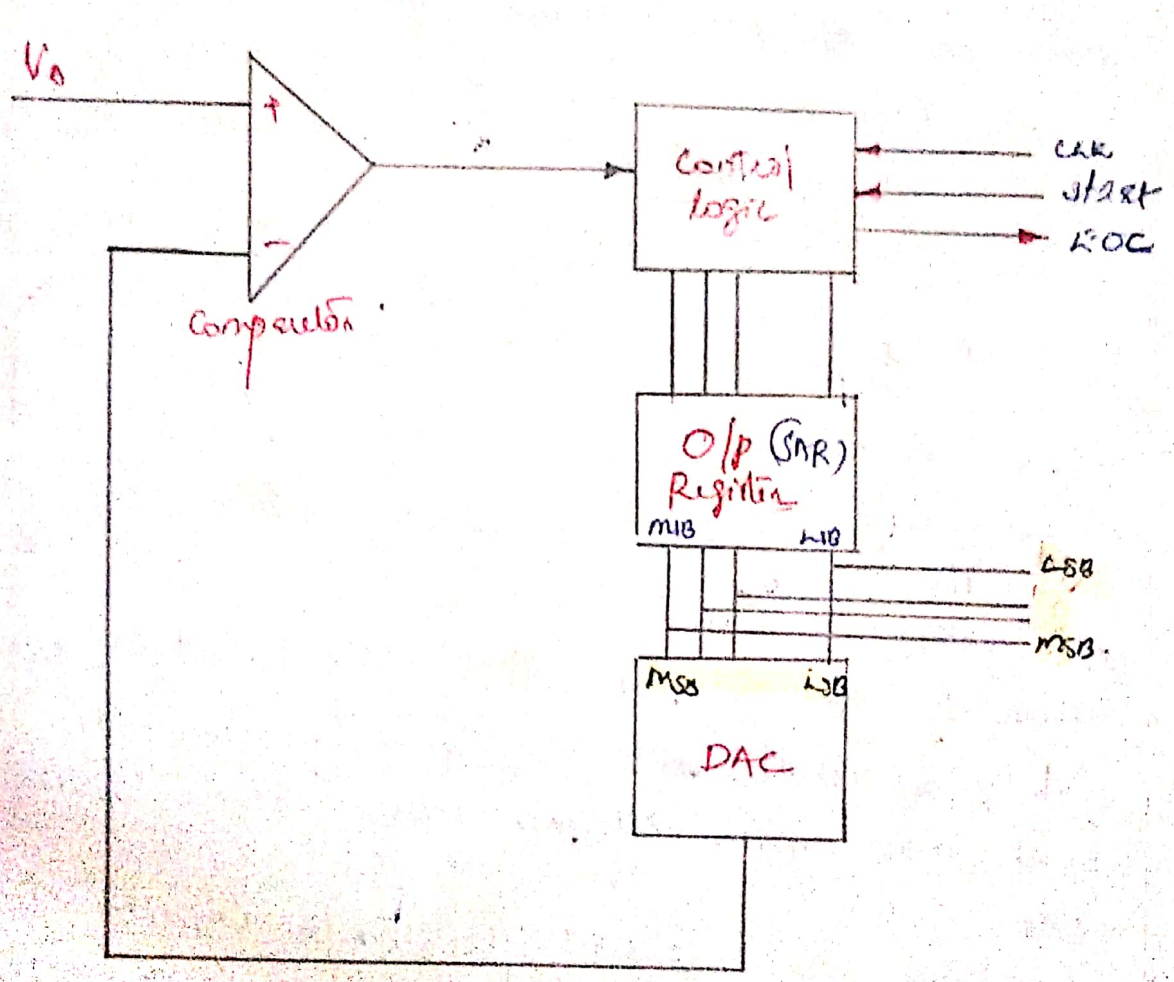
It is an integrating type ADC. The basic principle of integrating type ADC is that the voltage received by ramp controls the length of time that the binary counter is allowed to count. Thus a binary number proportional to value of Vin is obtained. In dual slope ADC two integrations are performed.



Here assume that counter is reset and o/p of integrator is zero. A conversion begins with the switch connected to analog input, so o/p of integrator is a +ve going ramp. Comparator o/p will be high and clock pulse will reach binary counter and counting starts. After 2^n clock pulses MSB of counter goes high & at next +ve clk edge goes high. At that time counter is reset and switch is connected to reference voltage Vref having polarity opposite to that of analog input.

Therefore o/p of integrator is -ve going ramp. AND gate is enabled and counter starts counting when ramp reaches 0V comparator switches to low stop clock pulses and counter. The count in the counter is proportional to time required for -ve ramp to reach zero, which is proportional to the voltage present during first integration which in turn proportional to analog input.

Successive Approximation type ADC



An SAR type ADC consists of a DAC, comparator & SAR (o/p register). The external clock input set internal timing parameter. The control signal start of conversion (SOC) initiates an A/D conversion process and

End of conversion is activated when conversion is completed (EOC).

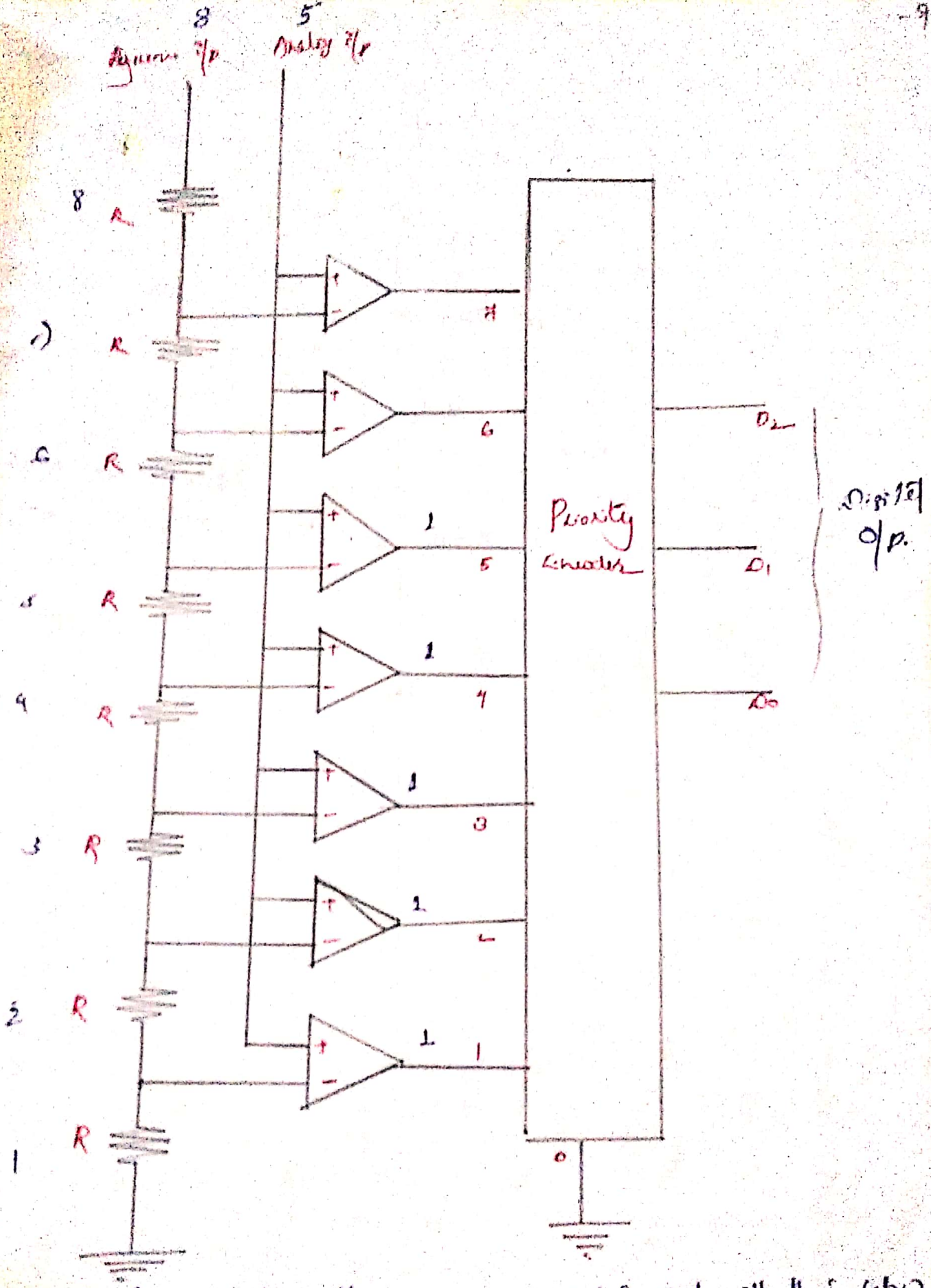
V_{in} is applied at one input of comparator. On receiving SOC signal control logic sets MSB bit to 1. The DAC converts the digital code to its equivalent analog signal and is connected to another input to comparator. Comparator compares these voltages and if input voltage V_{in} is greater than o/p of DAC MSB bit is kept MSB as 1 and sets next significant bit otherwise reset MSB as 0 and sets next significant bit as 1. The system enables the MSB first, then next significant bit and so on. After all bits of SAR have been fixed one conversion cycle is complete.

Conversion time $t_c = T(n+1)$ $T \Rightarrow$ clock period, $n \Rightarrow$ number of bits

FLASH ADC

These are high speed ADCs. Flash ADCs are also called Simultaneous or Parallel comparator ADC. because its fast conversion speed is achieved by providing $2^n - 1$ comparators and simultaneously comparing input signal with unique reference voltage levels. Speed limited by speed.

Figure shows 3 bit flash A/D converter. For this ADC $2^3 - 1$ comparators are required. One input of each comparator is connected to the input signal and other input to the reference voltage level generated by reference voltage divider.



For any given analog i/p on comparators and all those below it will have high o/p. All comparator o/p are connected to priority encoder, which produces a digital o/p corresponding to i/p having highest priority which in this case is the one that

represents largest input. Then the digital o/p represents the voltage that is closest in value to analog input.

Voltage applied to inv. terminal of uppermost comparator

$$\frac{7R}{7R+R} \times V_{ref} = \frac{7}{8} V_{ref}$$

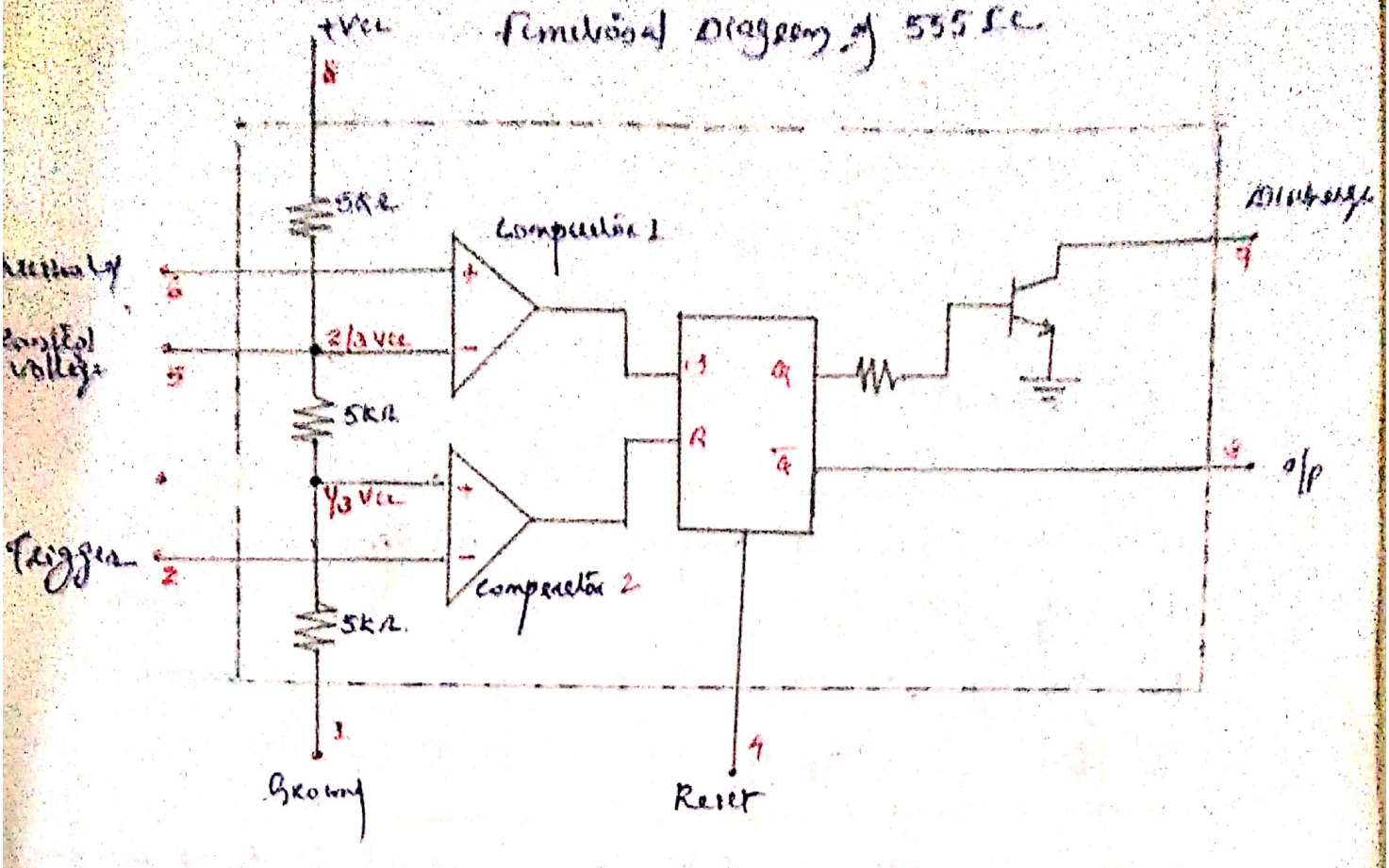
Voltage applied to inv. terminal of 2nd comparator from top

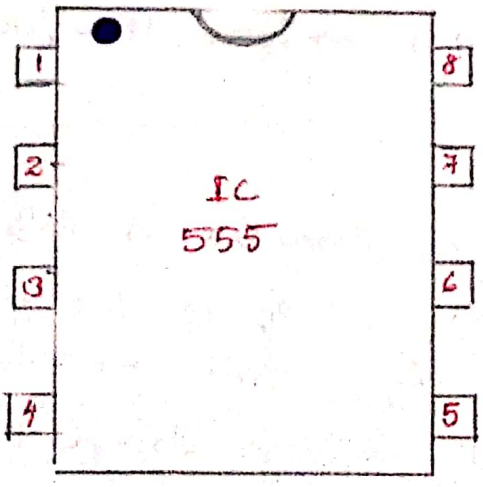
$$\frac{6R}{7R+R} \times V_{ref} = \frac{6}{8} V_{ref}.$$

Main drawback is its complexity. For 3 bit resolution, 7 comparators and 8 bit priority encoder are required.

555 Timer IC

Functional Diagram of 555 IC





Pin 1 : Ground : All voltages are measured with respect to this terminal.

Pin 2 : Trigger : IC 555 uses two comparators. The voltage divider consists of 3 equal resistances. One is voltage divider, voltage of non-inverting terminal of comparator 2 is Vcc/3. Inverting input of comparator 2 is compared with Vcc/3. When trigger i/p > Vcc/3 comparator 2's o/p becomes high and this resets the F/F.

Pin 3: Output: It is the complementary signal o/p ($\bar{Q}$) of F/F.

Pin 4: Reset: when pin 4 is grounded, it stops working of device and makes it off.

Pin 5: control voltage input:

This pin is the inverting terminal of comparator 1. The voltage divider holds voltage of this input $\frac{2}{3}V_{cc}$.

Pin 6: Threshold:

This is the non-inverting terminal of comparator 1. when the threshold voltage is more than $\frac{2}{3}V_{cc}$, comparator 1's o/p goes high. This is given to set input of RS flip-flop. ∴ it sets the F/F. ∴ Q output High & $\bar{Q}$ low ∴ o/p of IC at pin 3 is low.

For Threshold $> \frac{2}{3}V_{cc}$ F/F → Set Q → High o/p at pin 3 → low
For Trigger $< \frac{1}{3}V_{cc}$ F/F → Reset Q → low o/p at pin 3 → high

Pin 7: Discharge:

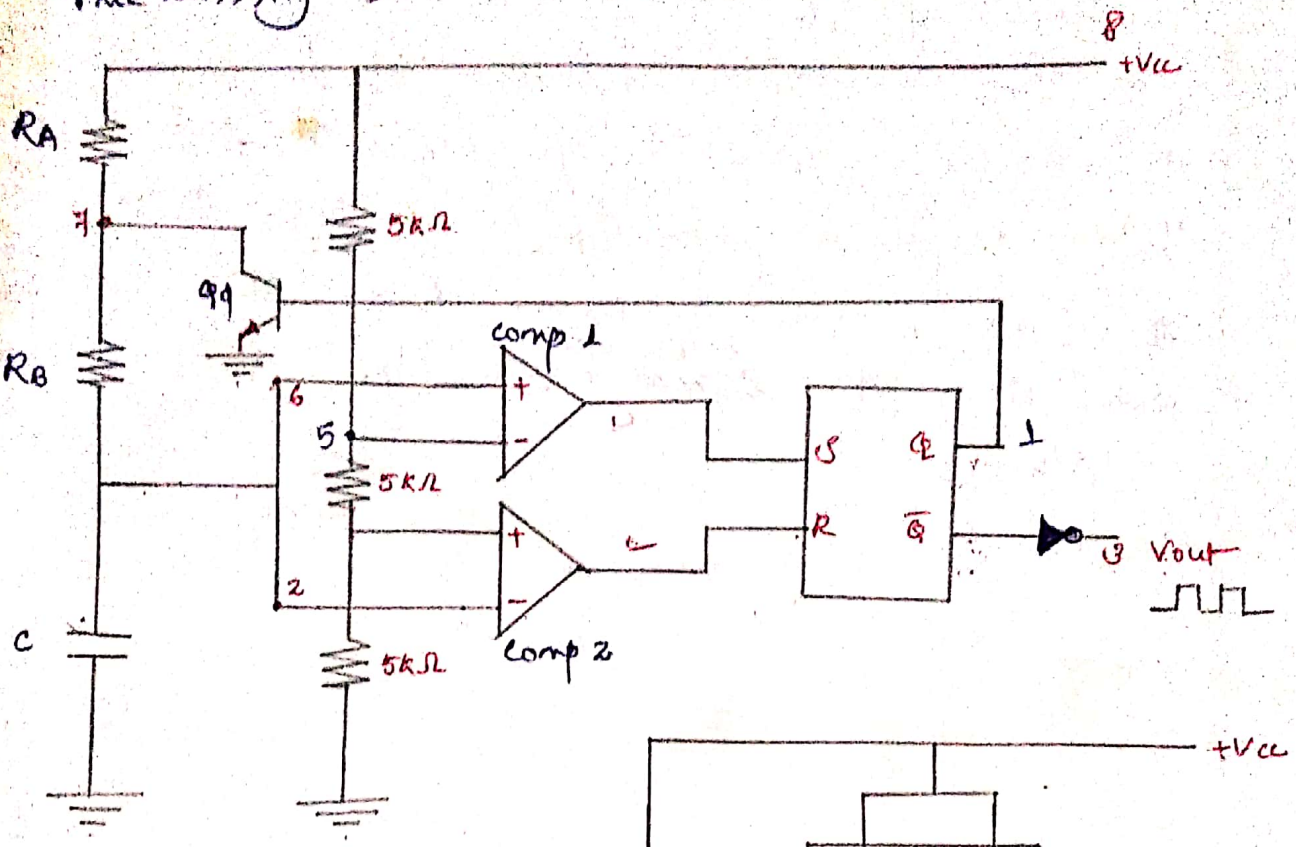
This pin is connected to collector of discharge transistor Q_1. when the o/p is low; Q is high which drives base of Q_1 high and provides a path to external capacitor to discharge through it.

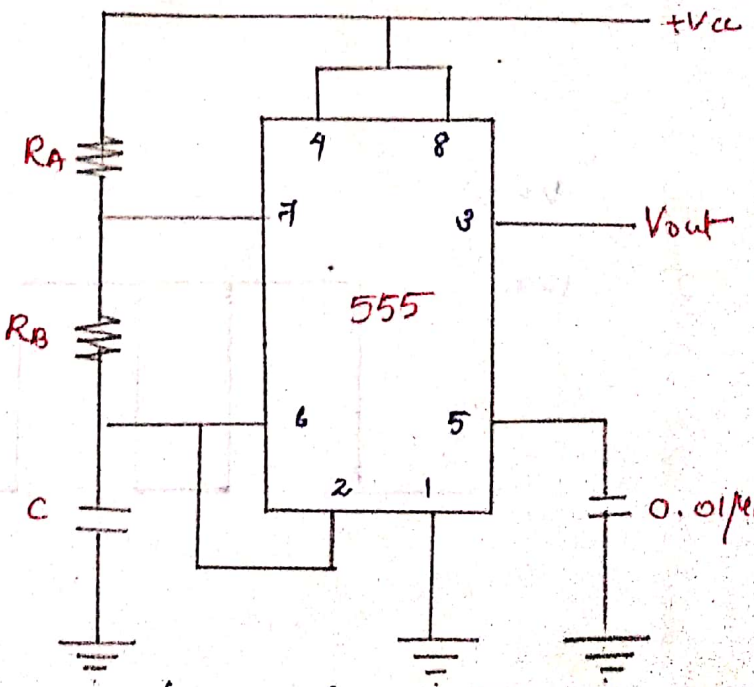
Pin 8: +Vcc

555 IC can work with any Supply voltage between 4.5V and 16V.

Astable Multivibrator Using 555

AMV is a Square wave Generator. It is also called Free running MV.



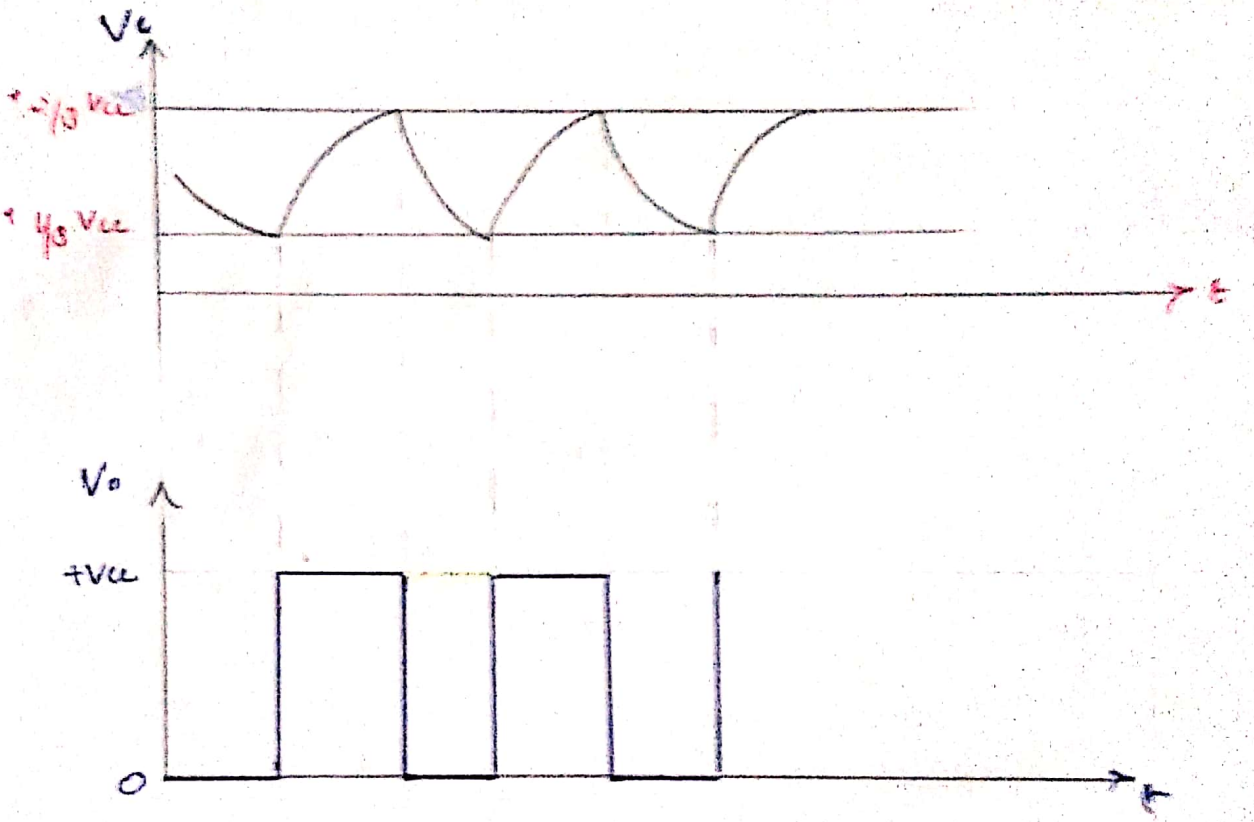


When F/F is set Q is high Q1 is in saturation and capacitor C gets discharged. While discharging when it becomes less than 1/3 Vcc, comparator 2's o/p goes high. This resets F/F and Q goes low & Q̄ high.

The low Q makes transistor off. Then capacitor starts charging through RA & RB. to Vcc

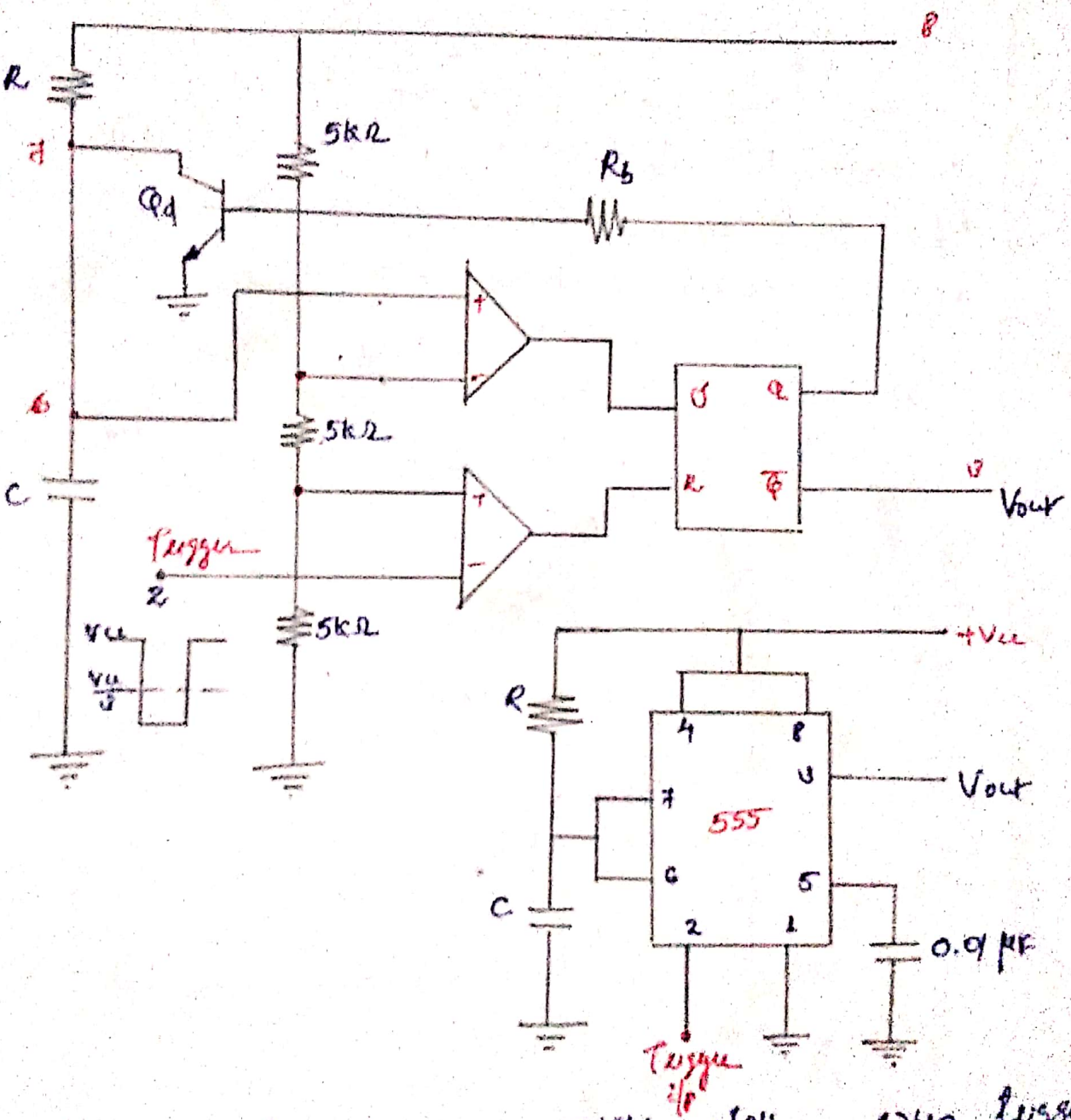
while charging capacitor voltage increases and when it exceeds $\frac{2}{3}V_{cc}$ o/p of comparator 1 goes high which sets F/F. Q becomes high and $\bar{Q}$ becomes low i.e. o/p or V_o is becomes low.

At this a diode transistor Q1 is saturated and capacitor discharges when voltage across it goes below $\frac{1}{3}V_{cc}$ comparator 2's o/p becomes high & F/F resets Q becomes low & $\bar{Q}$ becomes high. This cycle repeats and we get rectangular wave o/p.



Monostable Multivibrator Using 555 IC

555 IC can be operated as mono by connecting an external resistor and a capacitor as shown in figure



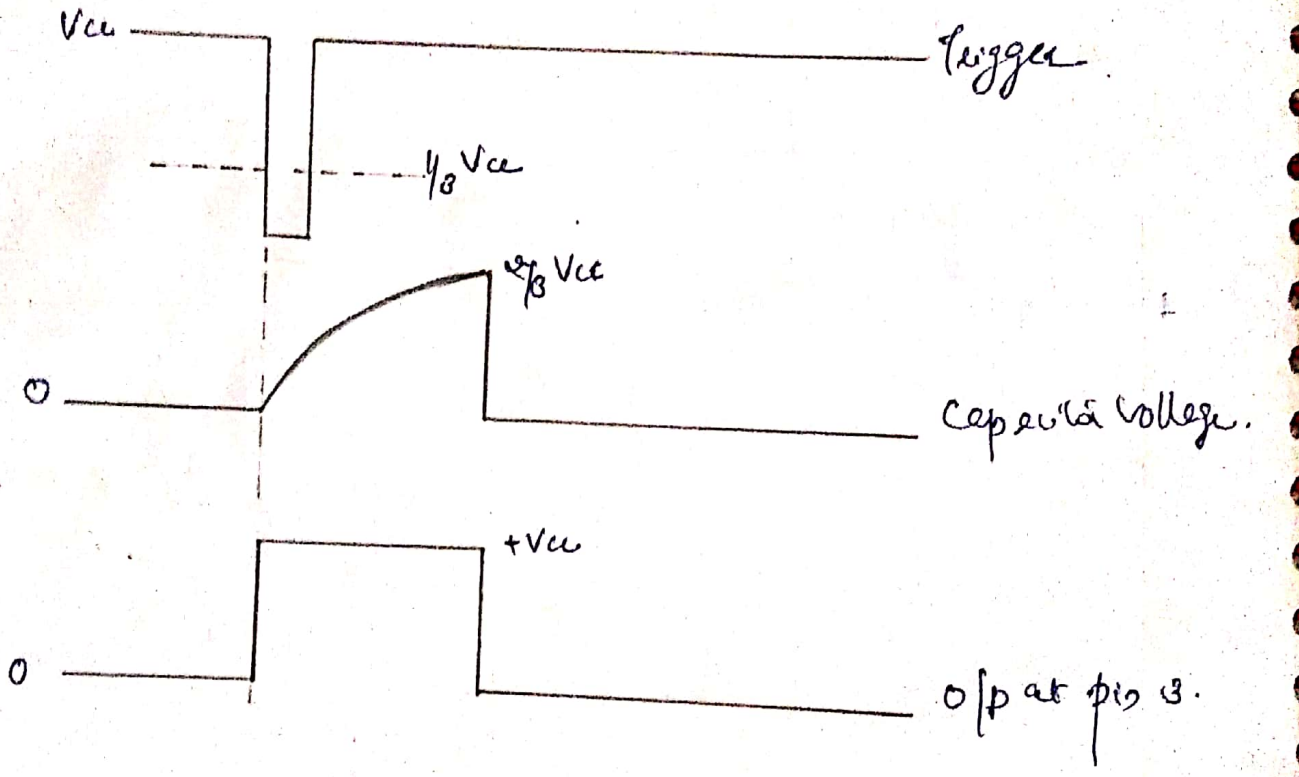
The ckt has only one stable state. When trigger applied, it produces a pulse in the output and returns back to its stable state. The duration of pulse depends on the values of R & C.

The F/F is initially set & Q is high it drives Q_1 to saturation & C is in discharged state

(-ve going pulse)

when trigger ↑ is applied at the start stable remains unchanged until trigger pulse is greater than $\frac{1}{3}V_{cc}$. when it becomes less than $\frac{1}{3}V_{cc}$ comparator 2's o/p goes high this resets F/F so Q goes low & $\bar{Q}$ & o/p at pin 3 becomes high. low Q makes transistor Q_d to off. Hence capacitor starts charging through R.

when voltage across capacitor becomes greater than $\frac{2}{3}V_{cc}$ comparator 1's o/p goes high. this set F/F. & Q becomes high & $\bar{Q}$ becomes low. drives Q_d to saturation & capacitor quickly discharges to zero.



Problems:

1) Design a LPF having cutoff frequency of 1kHz with pass band gain of 1.5.

Sol:

cutoff freq $f_H = 1kHz = \frac{1}{2\pi RC}$

Let $C = 0.01\mu F$ (say)

$R = 7.95k\Omega \simeq 10k\Omega$.

Given pass band gain $A_f = 1.5 = 1 + \frac{R_f}{R_1}$

$\frac{R_f}{R_1} = 1.5$; $R_f = 1.5 R_1$

$\because R_1 \| R_f = R$; $\frac{R_f R_1}{R_f + R_1} = 10k\Omega$

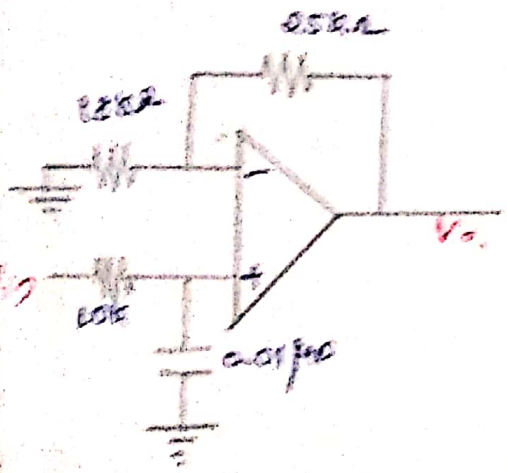
$\frac{1.5R_1 \times R_1}{1.5R_1 + R_1} = 10k\Omega$

$\frac{1.5R_1^2}{2.5R_1} = 10k\Omega$

$R_1 = 16.66k\Omega \simeq 18k\Omega$

(say) $R_f = 16.66k \times 1.5$

$= 25k\Omega$



2) Design a 2nd order LPF at high cutoff frequency 1kHz.

For Butterworth Response gain $A_f = 1.586$

$f_H = 1kHz = \frac{1}{2\pi RC}$; $C = 0.01\mu F$

$R = 15.92k\Omega \simeq 16k\Omega$

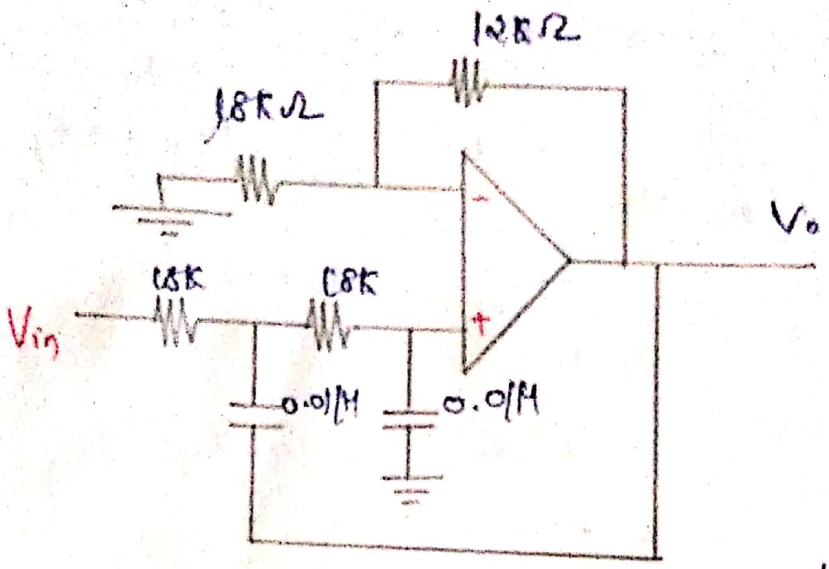
$1 + \frac{R_f}{R_1} = 1.586$

$\frac{R_f}{R_1} = 0.586$

If $R_1 = 18K\Omega$; $R_f = 18K \times 0.586 = 10.55K\Omega \simeq 12K\Omega$

Then required components are

$R = 18K\Omega$, $R_1 = 18K\Omega$, $R_f = 12K\Omega$; $C = 0.01\mu F$



3) Design a LPF having cutoff frequency of 1KHz and pass band gain 2.

4) Determine the resolution of
   (a) 6 bit DAC
   (b) 12 bit DAC in terms of percentage.

(a) For 6 bit DAC

$$\% \text{ Resolution} = \frac{1}{2^N - 1} \times 100 = \frac{1}{2^6 - 1} \times 100$$

$$= \frac{1}{63} \times 100$$

$$= 1.587\ \%$$

(b) For 12 bit DAC

$$\% \text{ Resolution} = \frac{1}{2^{12} - 1} \times 100 = 0.0244\ \%$$

5) A 6 bit DAC has step size of 50mV. Determine full scale o/p voltage and % resolution.

Given 6 bit Number of steps = $2^6 - 1 = 63$.

Full scale o/p = Step size × Number of steps

$$= 63 \times 50\text{mV}$$

$$= 3.15\text{V}$$

$$\% \text{ Resolution} = \frac{\text{Step size}}{\text{Full scale o/p}} \times 100 = \frac{50\text{m}}{3.15} \times 100$$

$$= 1.587\ \%$$

6) On 8 bit DAC produces Vout = 0.05V for a digital input of 00000001. Find full scale o/p. what is its resolution? what is Vout for an input 00101010?

Full scale o/p = Step size × Number of steps

$$= 0.05 \times 2^8 - 1 = 12.75\text{V}$$

% resolution = $\frac{1}{2^8 - 1} \times 100 = 0.392\%$

for an input of 00101010 o/p = 42 × 0.05

= 2.10V

3) Design a 4 bit weighted resistor DAC whose full scale o/p voltage is −5V. logic levels are 1 = +5V & 0 = 0V. also find o/p voltage when input is 1101.

Full scale o/p

$$= -\left[D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8}\right]\frac{R_f}{R} = -5V$$

$$\left[5 + 5/2 + 5/4 + 5/8\right]\frac{R_f}{R} = 5$$

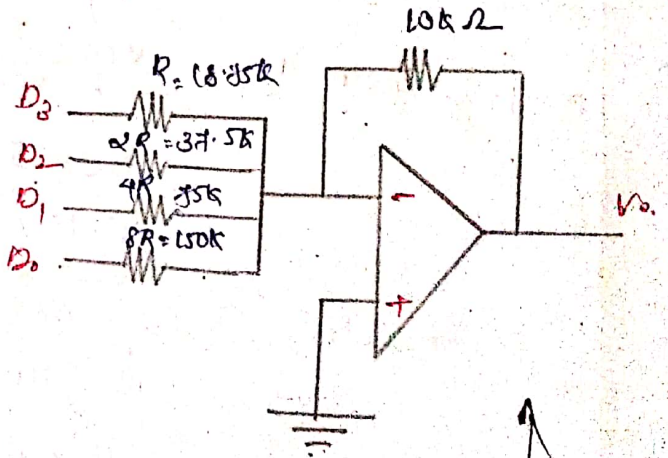
$$\frac{R_f}{R} = \frac{5}{9.375} = 0.533$$

$R_f = 10K\Omega$ $\quad R = 18.75\ K\Omega$

$\therefore$ $2R = 37.5\ K\Omega$

$4R = 75K\Omega$

$8R = 150\ K\Omega$



Sun 18/11/12

CONTENT BEYOND THE SYLLABUS

PCB DESIGN

Intro to PCB Design

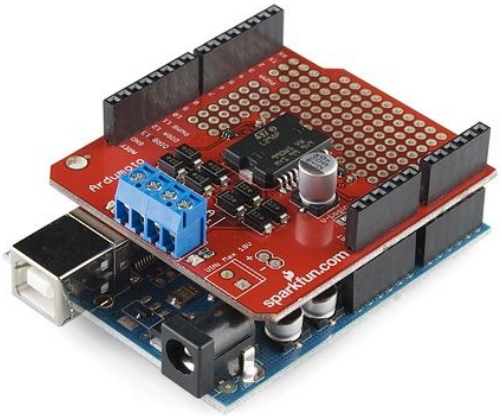
Objectives

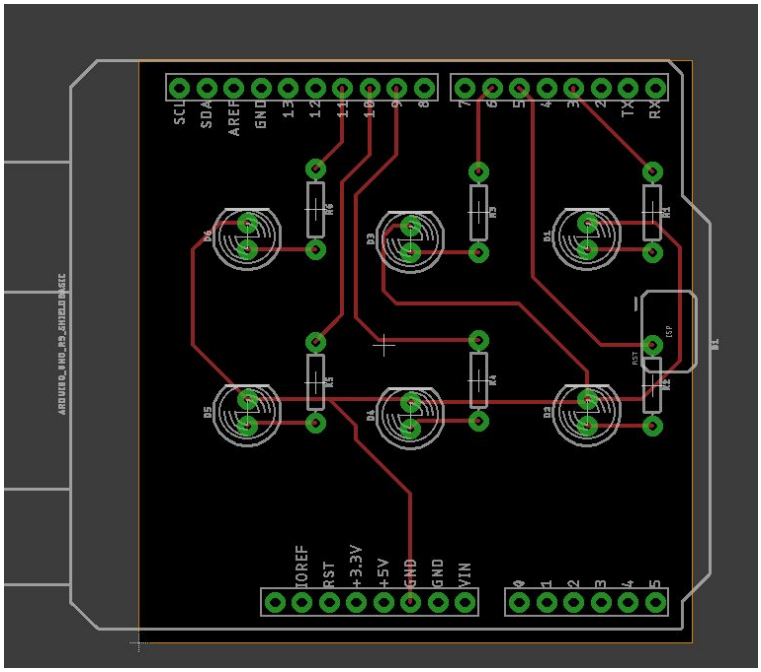
In this tutorial we'll design a printed circuit board (PCB) in Eagle. This PCB will be an Arduino shield - a board that sandwiches with an Arduino microcontroller to provide extra functionality. The PCB will have a collection of LEDs on it that can be controlled from the arduino.

- Get familiar with the process and vocabulary of PCB design
- Learn how to use Eagle
- Lay a foundation that you can build off of to do more complex PCB design in the future

You can learn more about Arduino shields here: https://learn.sparkfun.com/tutorials/arduino-shields/all

Questions? Email: katelyn.brinker@ieee.org or brinker@iastate.edu





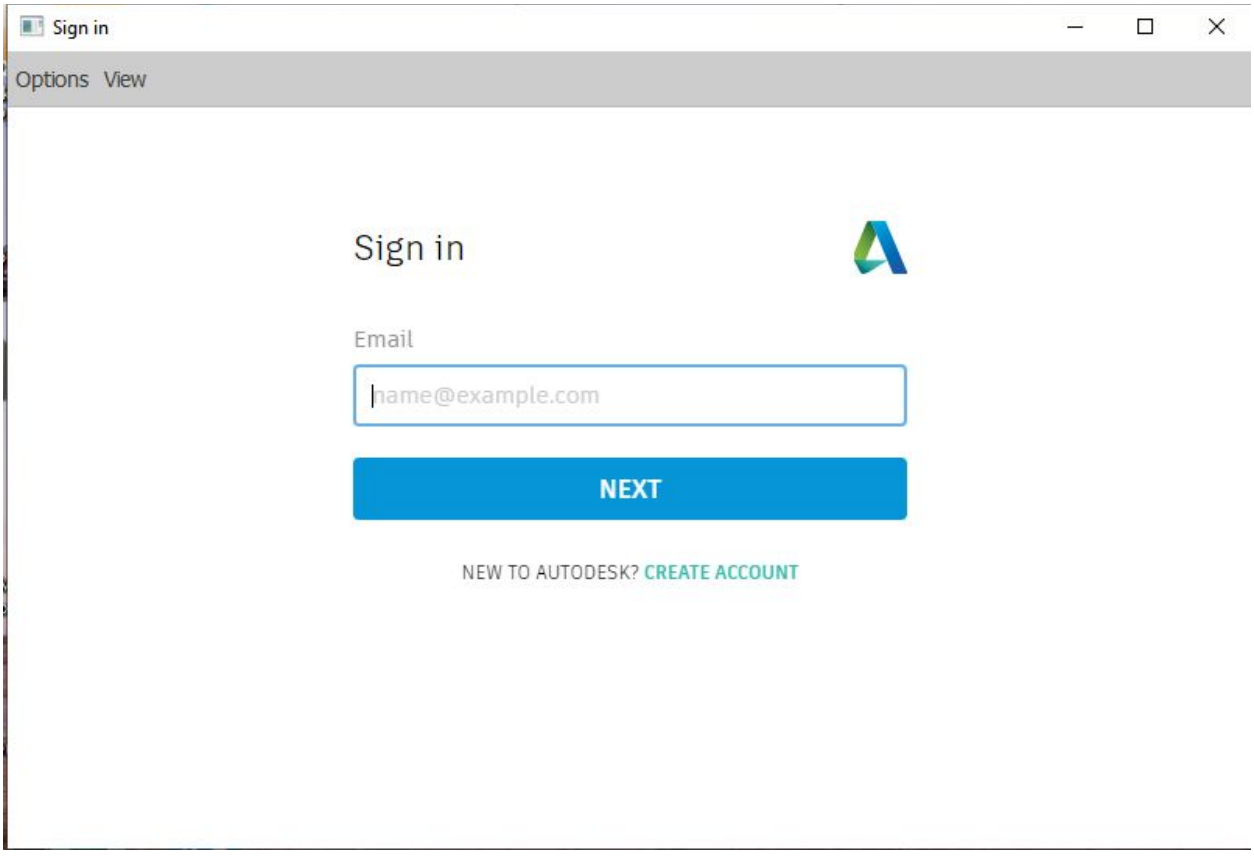
Getting Started

There are many different PCB design softwares, such as the following:

- Eagle
- Altium
- Cadence
- KiCAD
- CircuitMaker

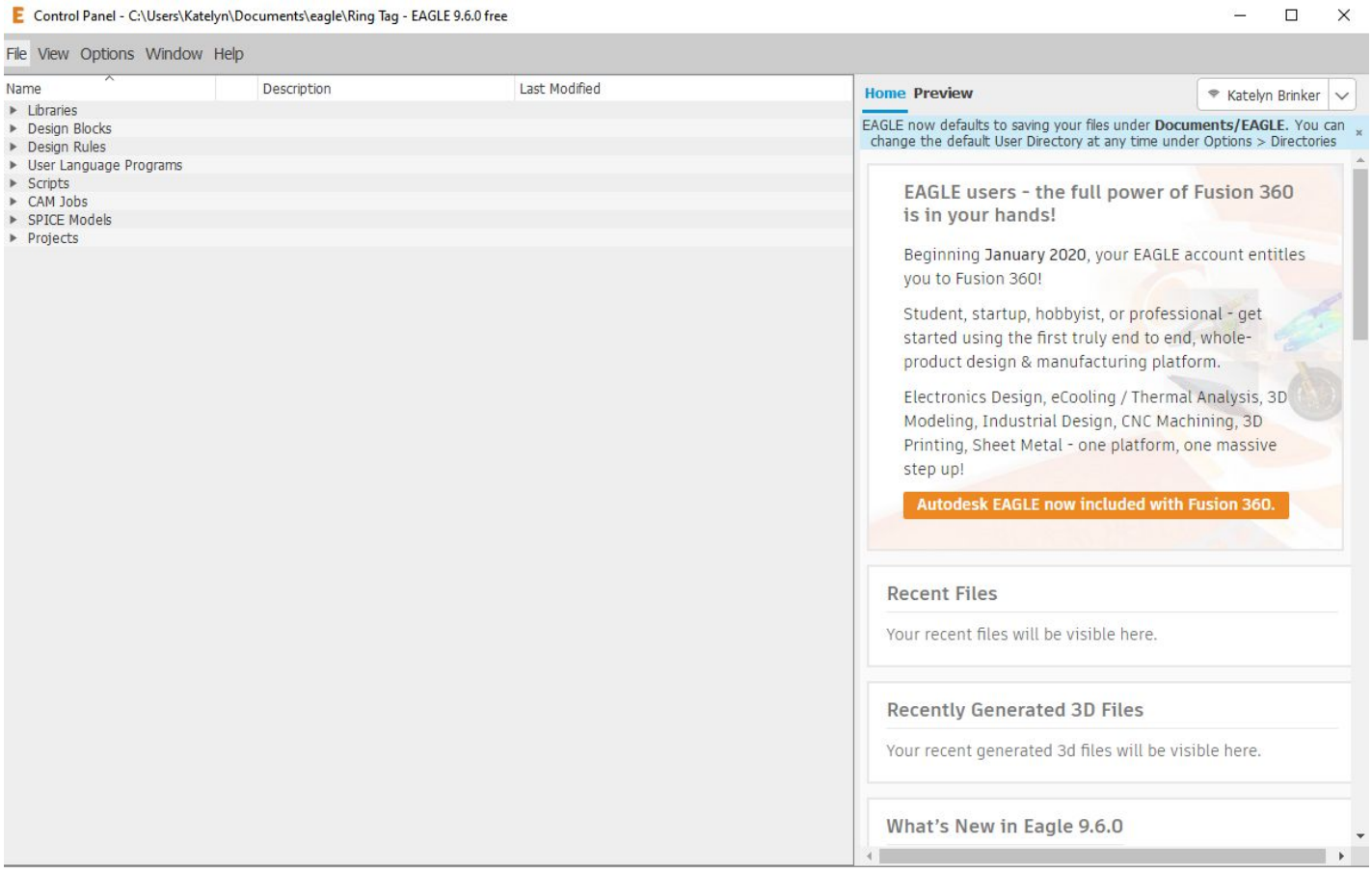
Eagle, KiCAD, and CircuitMaker have free versions. Altium and Cadence are both really powerful and customizable, but this makes them more difficult to learn on. The free version of Eagle is pretty user friendly and straightforward to learn on and provides the functionality we need for the workshop, so that's what we're going to use.

1. Download Eagle from the autodesk website: https://www.autodesk.com/products/eagle/free-download
2. After you download it, either create an Autodesk account or sign in with yours. After this is complete, Eagle will open in the Control Panel view.

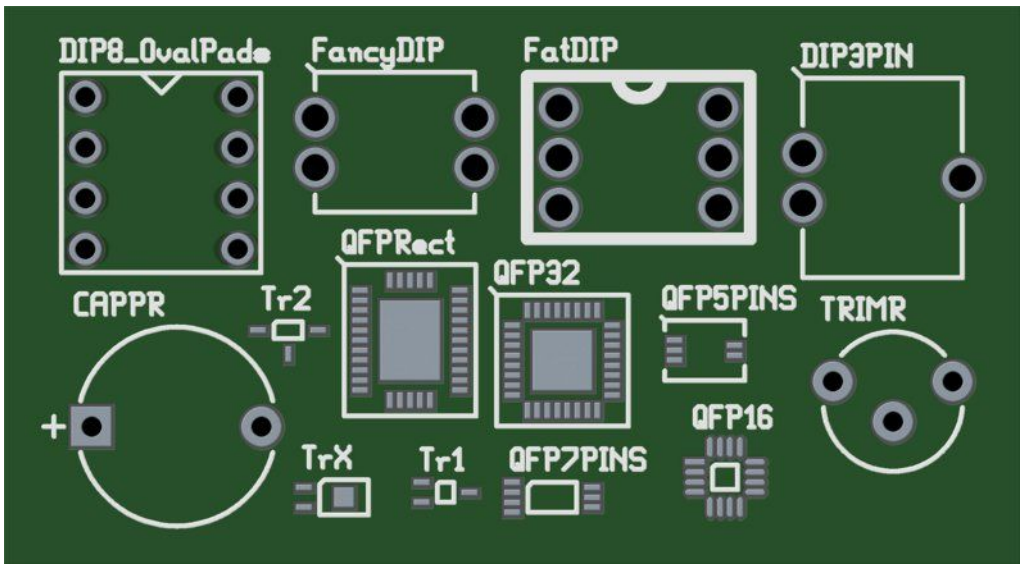


The Control Panel is your home base in Eagle. This is where you can create and access your projects and libraries.

Libraries are files that contain part descriptions: what is the symbol that represents the part and what does the part's physical footprint need to look like.

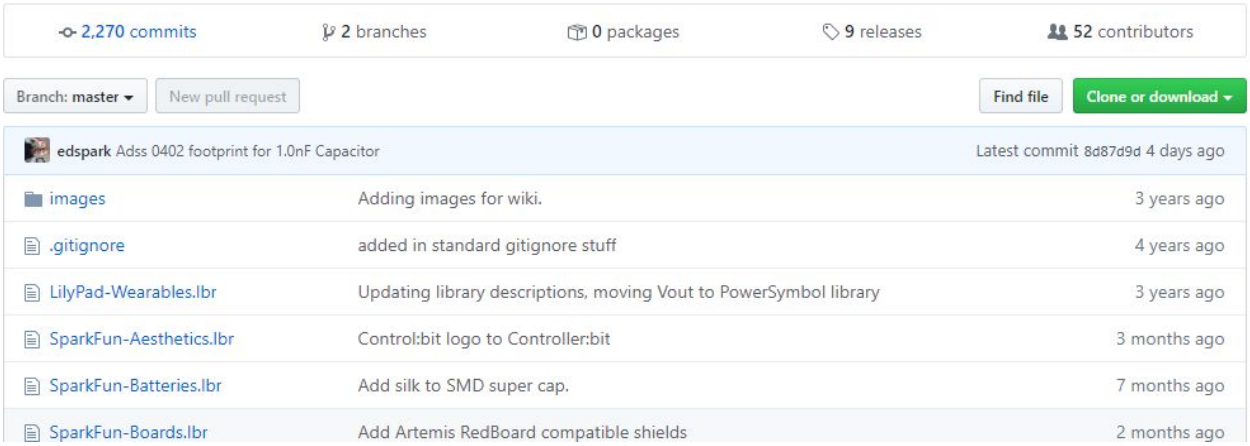


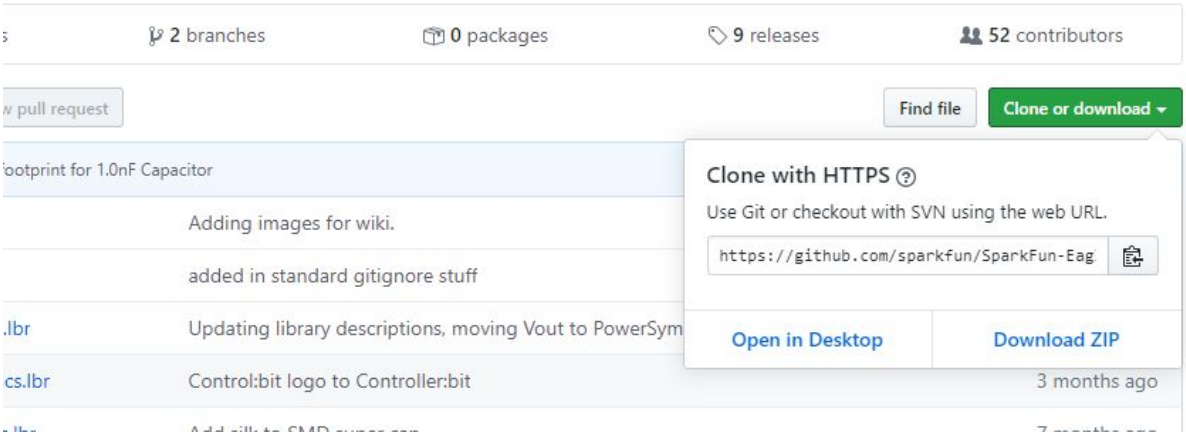
The footprint is the layout of the pads that the component will be soldered to.



You can make your own libraries or you can download premade libraries. We're going to be using the SparkFun Eagle libraries that are on github.

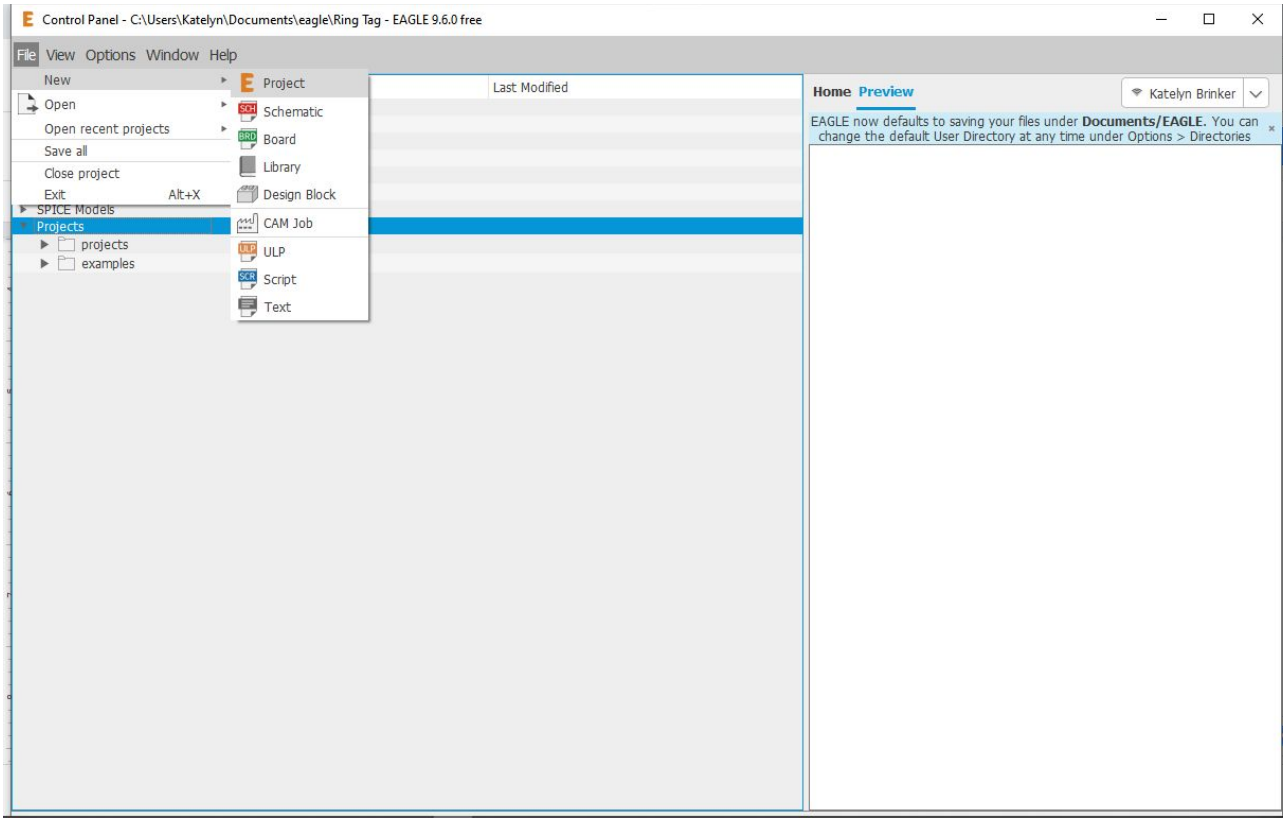
3. Download the SparkFun Eagle libraries from github using this link: https://github.com/sparkfun/SparkFun-Eagle-Libraries Click on "Clone or download" and then select "Download ZIP"
4. Extract the library files from the zip file.

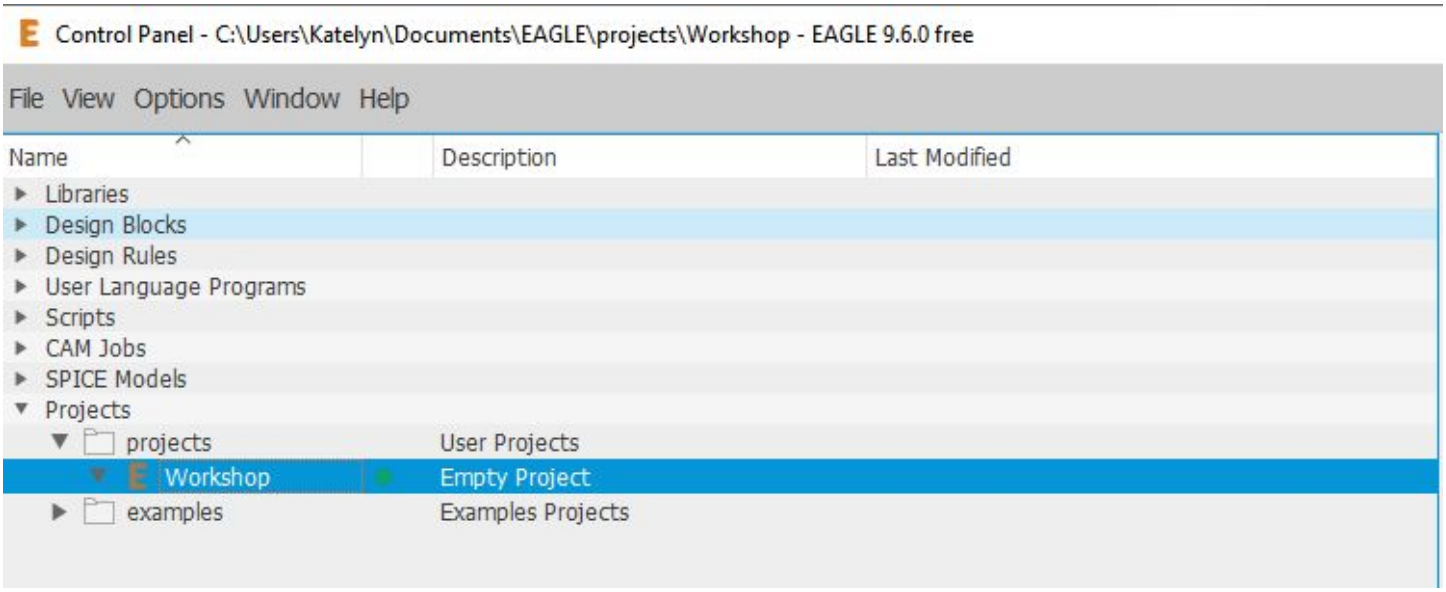




We'll include the libraries once we start laying out the schematic. But first, we need to start a "Project" for our board to reside in.

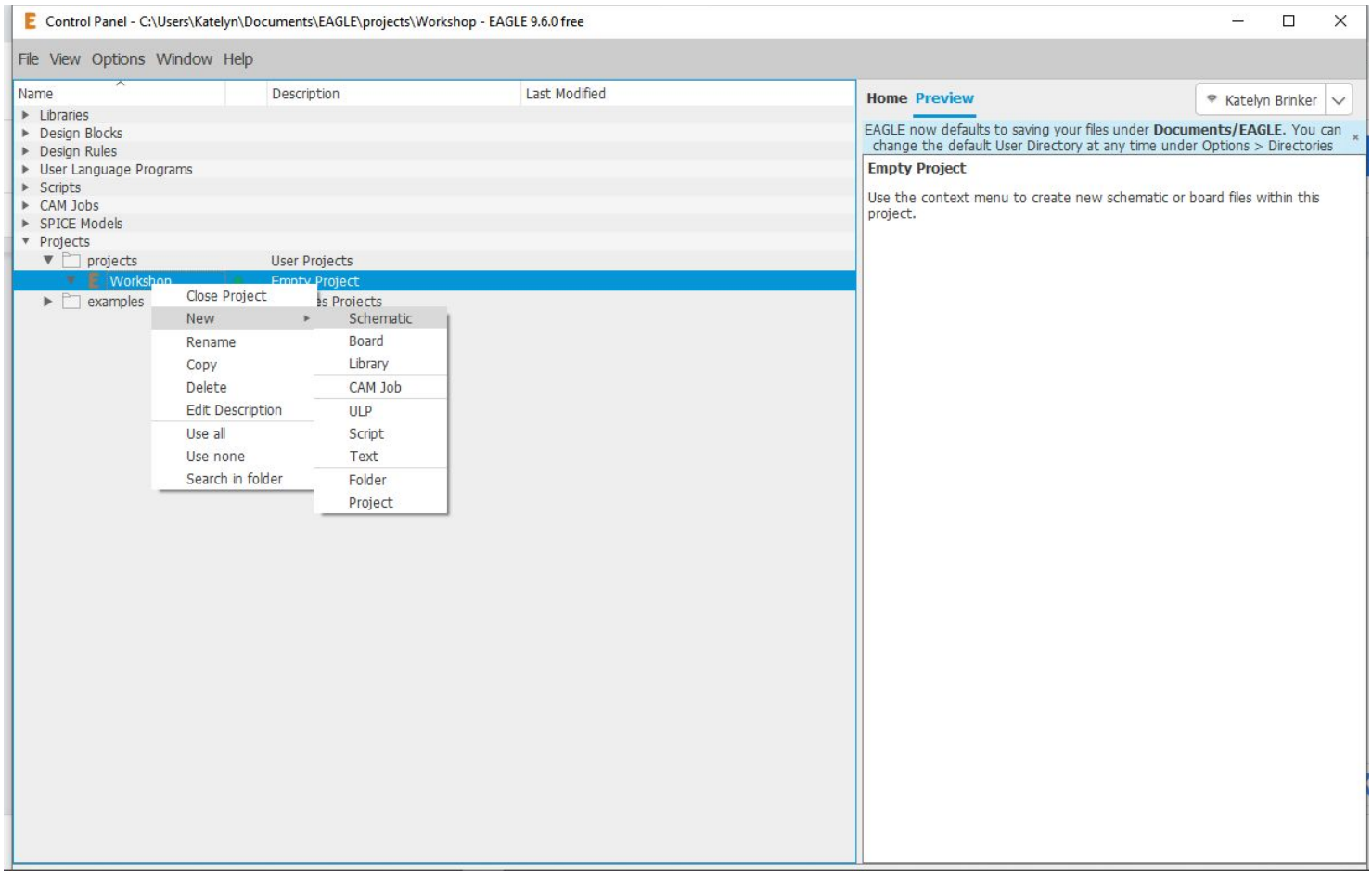
5. In the top menu of the Control Panel select File - New - Project. This will add a new project under the "projects" tab in the Control Panel. Rename the new project whatever you want. In this tutorial it is named "Workshop." The project description for the project you just created should be "Empty Project"

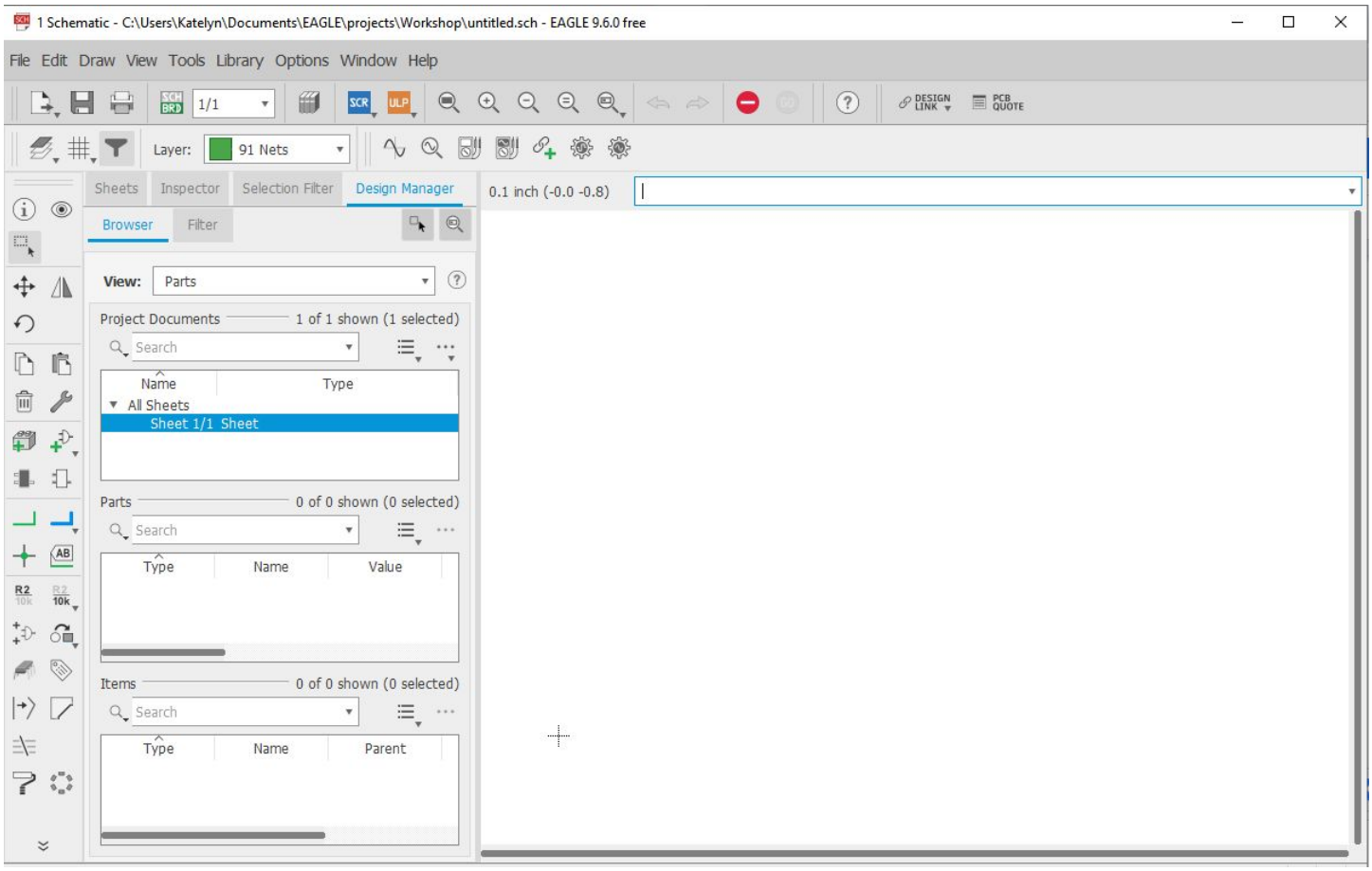




We'll add the schematic and layout to the project so that all the pieces we need for making a PCB are grouped together.

6. Right click on your project in the Control panel then select New - Schematic. A schematic will then be added to your project and will open in a new window.


Control Panel - C:\Users\Katelyn\Documents\EAGLE\projects\Workshop - EAGLE 9.6.0 free
File View Options Window Help
Name
Description
Last Modified
Libraries
Design Blocks
Design Rules
User Language Programs
Scripts
CAM Jobs
SPICE Models
Projects
projects
User Projects
Workshop
Empty Project
examples
Close Project
New
Rename
Copy
Delete
Edit Description
Use all
Use none
Search in folder
Schematic
Board
Library
CAM Job
ULP
Script
Text
Folder
Project
Home
Preview
Katelyn Brinker
EAGLE now defaults to saving your files under Documents/EAGLE. You can change the default User Directory at any time under Options > Directories
Empty Project
Use the context menu to create new schematic or board files within this project.


1 Schematic - C:\Users\Katelyn\Documents\EAGLE\projects\Workshop\untitled.sch - EAGLE 9.6.0 free
File Edit Draw View Tools Library Options Window Help
Layer:
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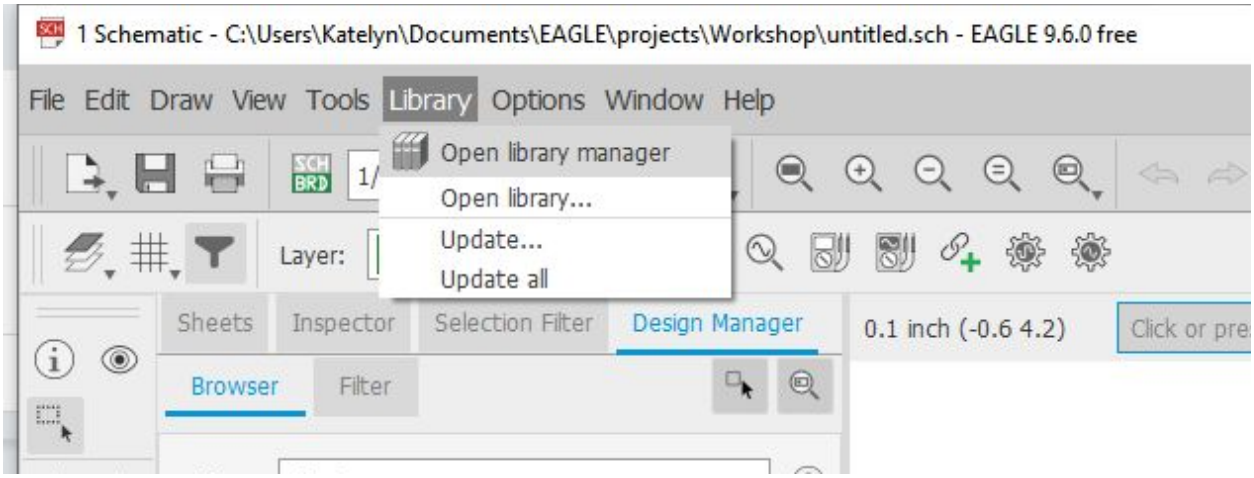
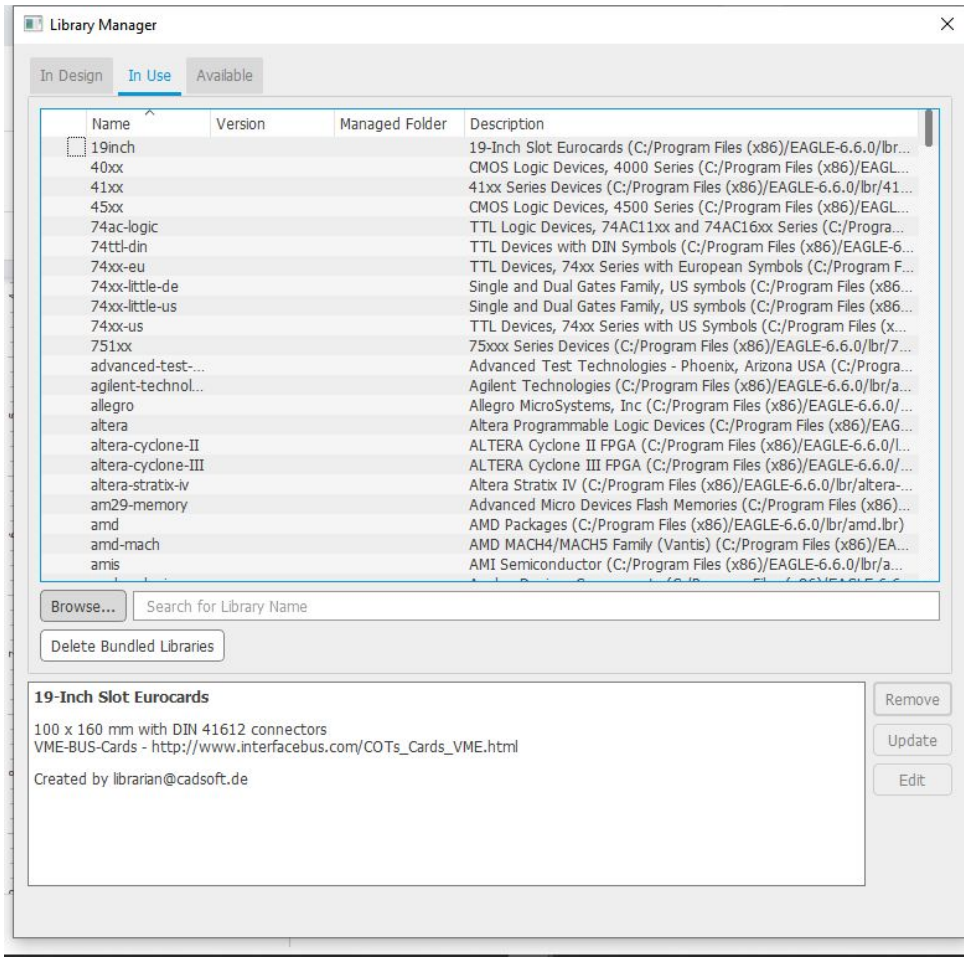
We're going to add the sparkfun libraries through the library manager before we layout the schematic.

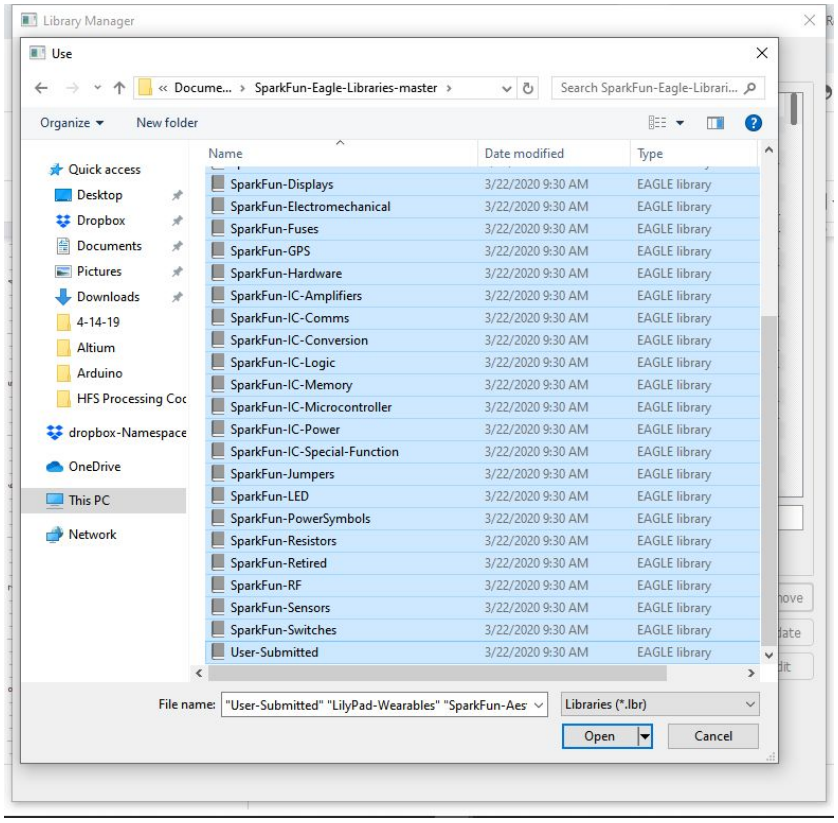
7. From the top menu select "Library" and then click on "Open library manager"



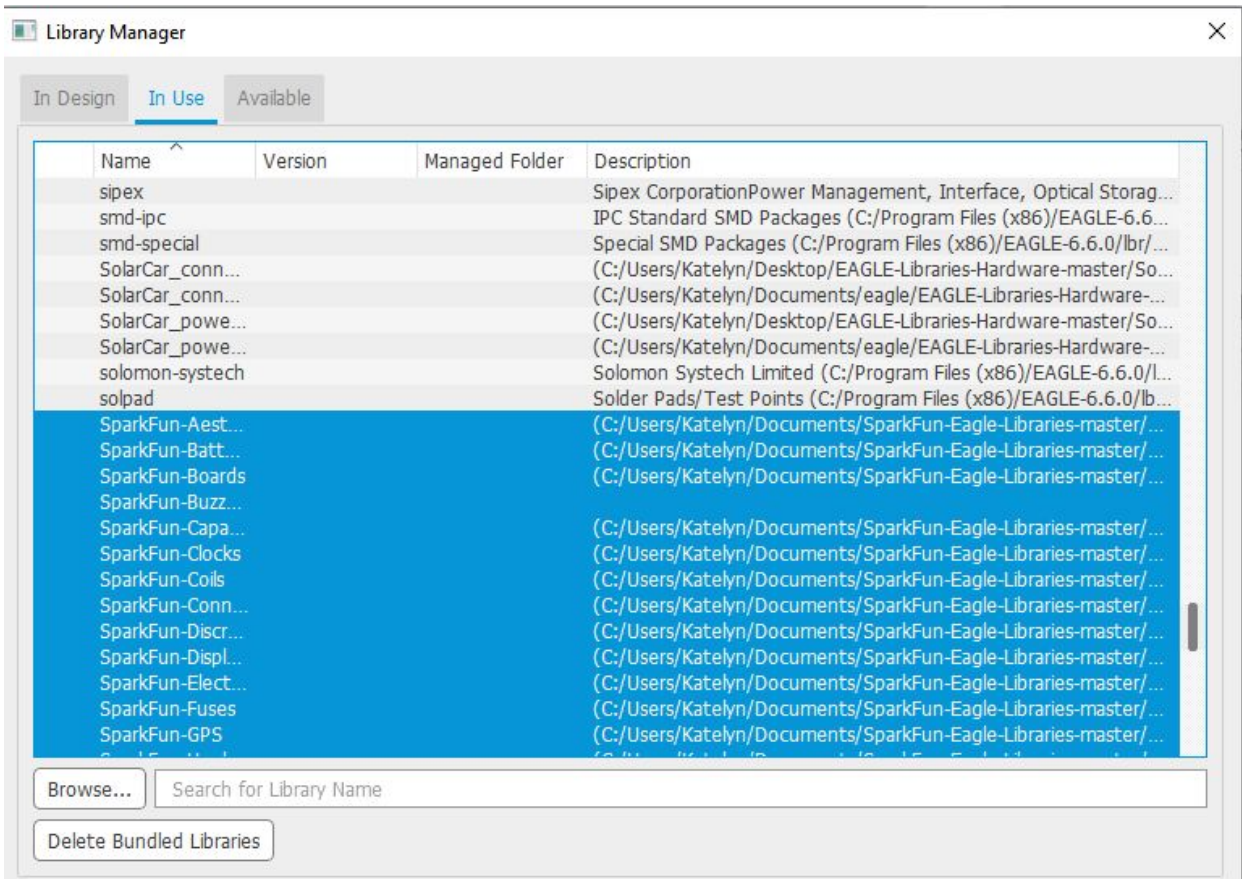
8. Navigate to the "In Use" tab of the Library Manager and then hit the "Browse" button.



9. In the pop up window, browse to where you extracted the SparkFun library files previously. Select all the individual library files and then hit the Open button.



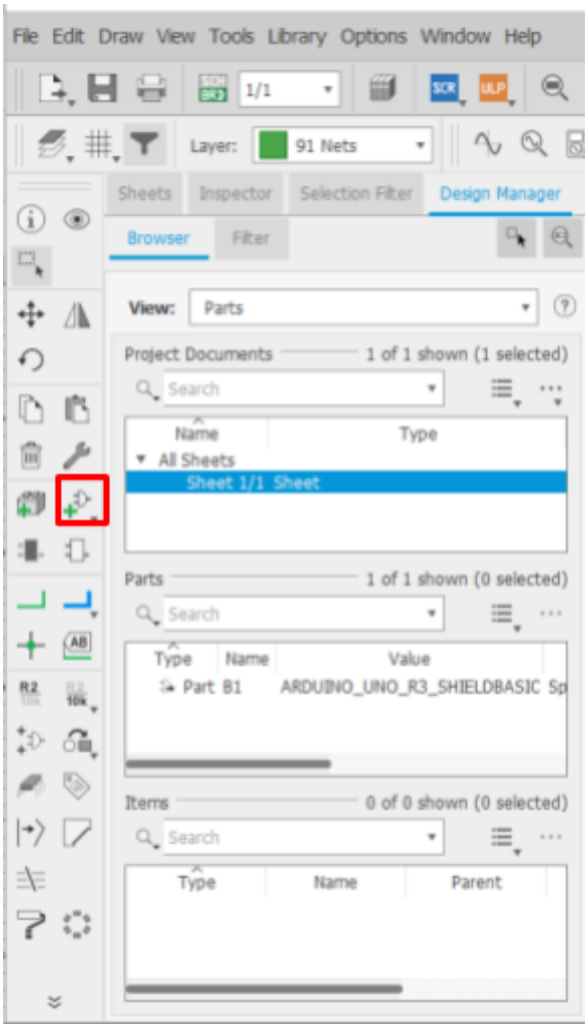
10. In the library manager under the “In Use” tab, scroll down and make sure the SparkFun libraries appear in the list.



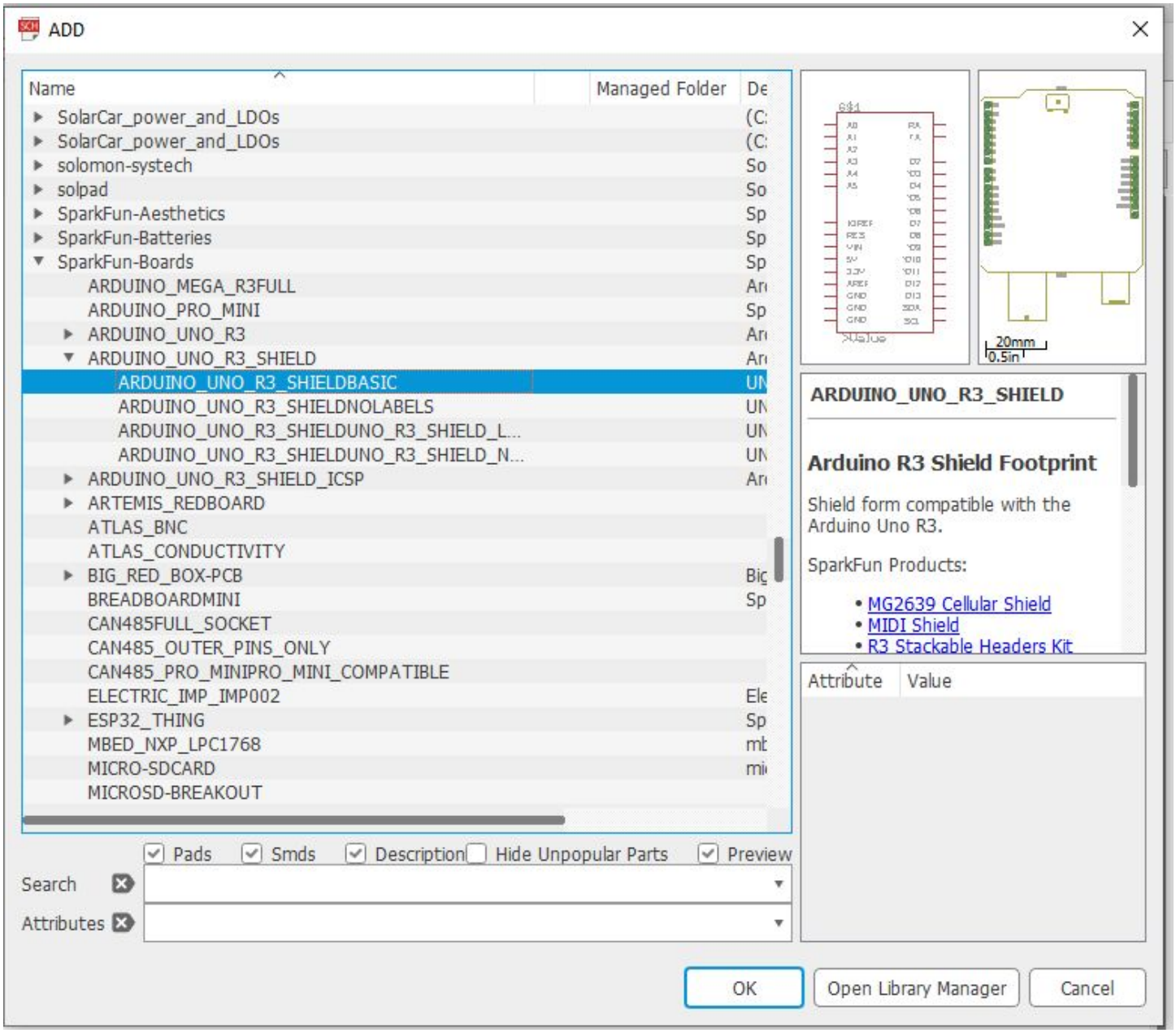
Schematic Layout

The schematic is the symbolic description of the PCB. It's analogous to a circuit diagram. It's where we'll indicate the connections between parts and it'll help us when we do the board layout later.

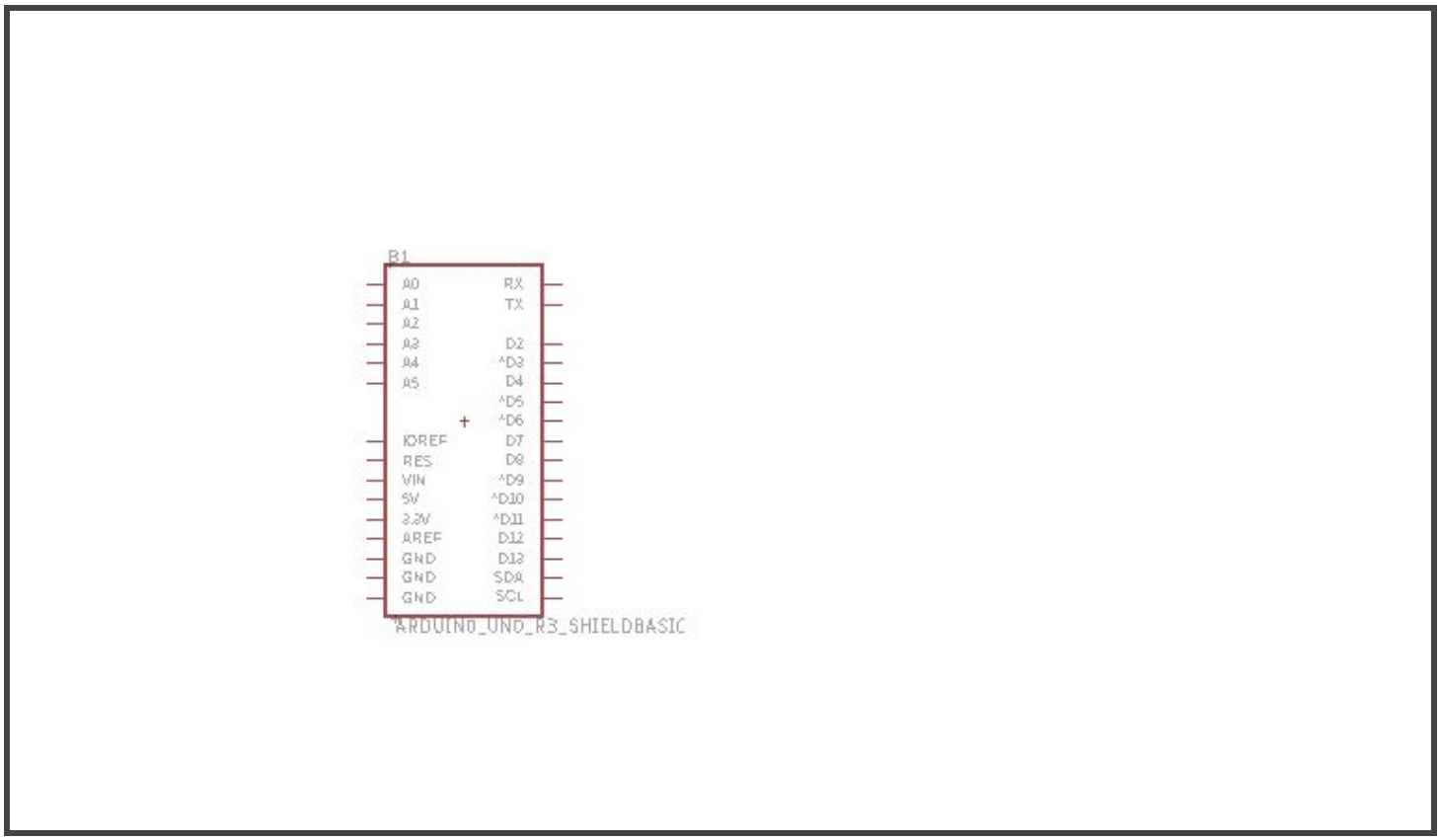
We'll use the tools in the toolbar on the left to build the schematic. The button to add components is boxed in red in the image below. Hovering over this tool brings up the description "Add Part"



11. Save your schematic by hitting the save button in the upper left or through File - Save
12. Click on the Add Part tool. In the Add window that pops up, navigate to SparkFun-Boards, then ARDUINO_UNO_R3_SHIELD, and then select ARDUINO_UNO_R3_SHIELDBASIC. A preview of the schematic symbol and footprint will show in the Add window. Select OK.



13. Place an instance of the Arduino Uno shield symbol in the schematic window by clicking once in the white canvas in the schematic window. Clicking again will place another instance of the symbol. Press the escape button on your keyboard to exit the symbol placement mode. This will bring you back to the Add window. Pressing escape again will close the add window.



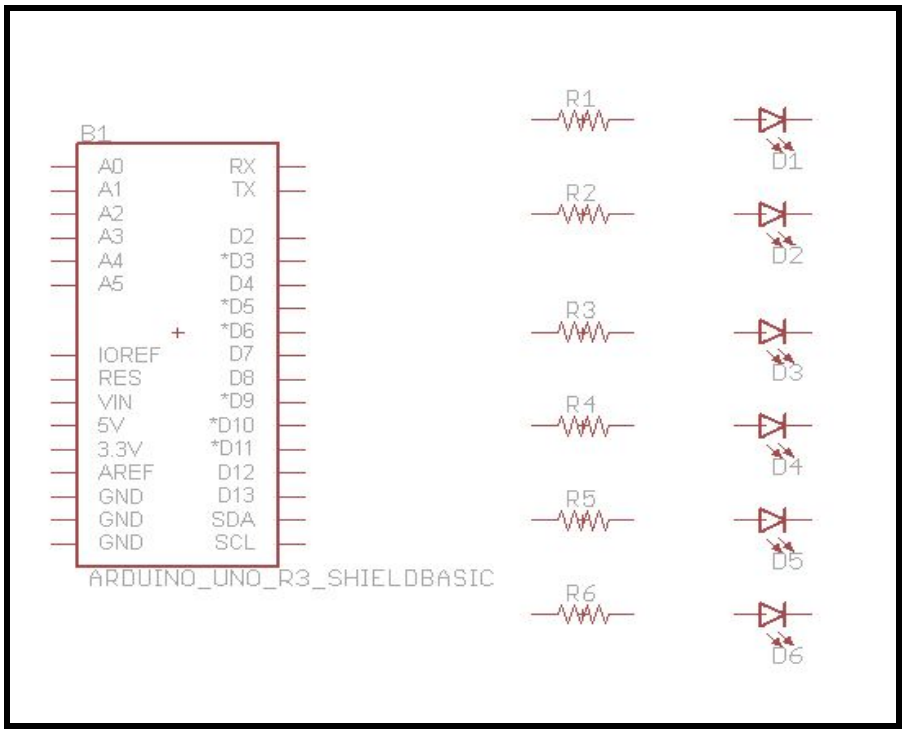
To pan the schematic canvas, hold down your mouse's scroll wheel and drag the canvas. To zoom in, roll the scroll wheel away from you. To zoom out, roll the scroll wheel towards you.

You can rotate a symbol by right clicking before you left click to place it in the schematic.You can also right click on the symbol and then select rotate.

14. Place the components in the BOM below in the schematic. The Library column tells you where to find the part in the Add window. Remember that you can right click before placing a component to rotate it. After placing components, you can use the move tool in the left hand toolbar to arrange the symbols nicely.

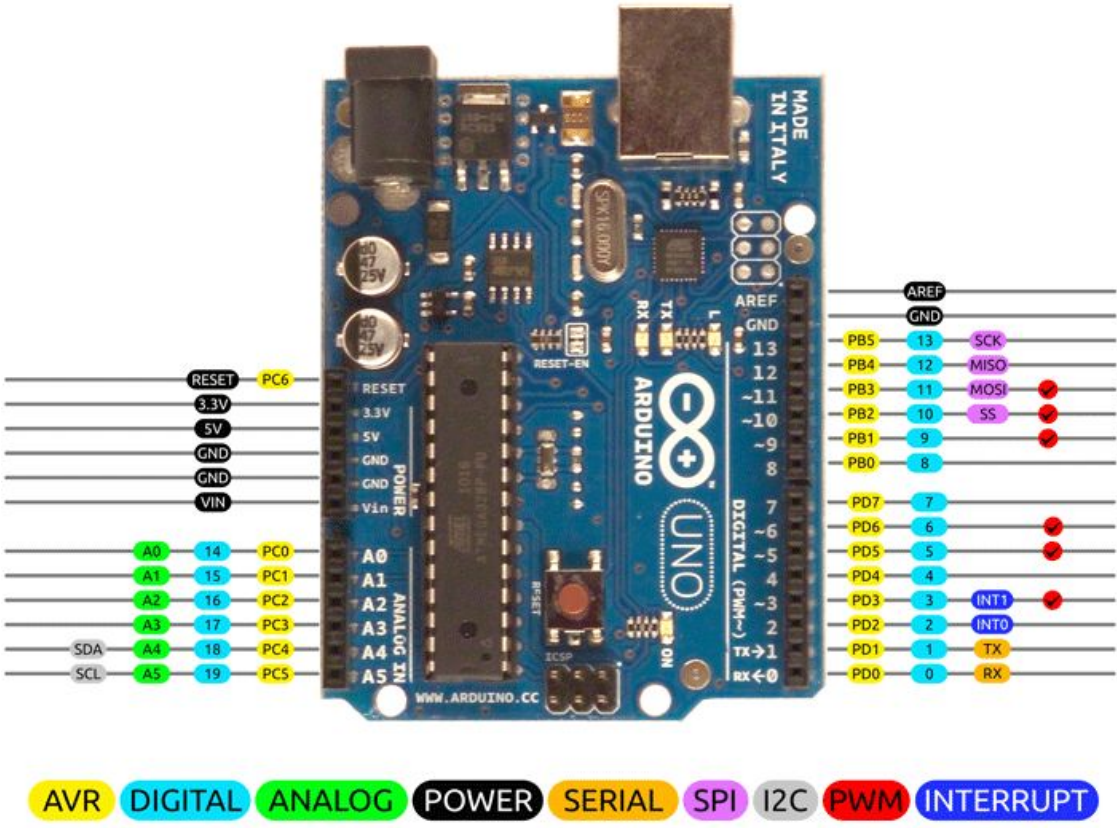
Bill of Materials (BOM)

Part Name	Library/Folder	Quantity
ARDUINO_UNO_R3_SHEILDBASIC	SparkFun-Boards -> ARDUINO_UNO_R3_SHIELD	1
RESISTORAXIAL-0.3	Sparkfun-Resistors ->RESISTOR	6
LED5MM	Sparkfun-LED ->LED	6



The resistors will be used to limit the current going into the LEDs. We want to connect each LED to a resistor and to a digital pin on the Arduino through the shield board. The full pinout of the Arduino is shown below. All the pins whose names start with “D” (e.g., D2 or D7) are digital pins.

Arduino Pinout

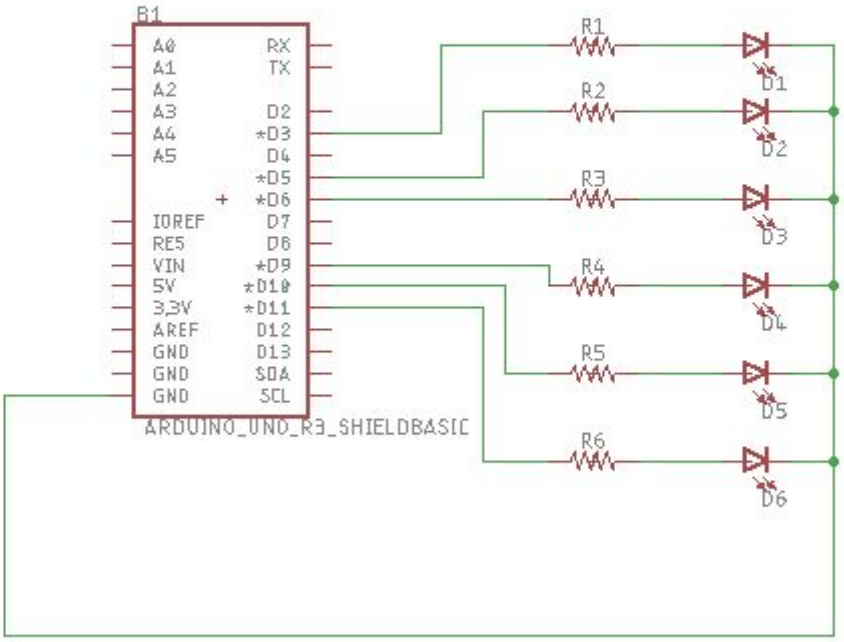


15. Use the Net tool (green L shape button) in the toolbar to connect the symbols according to the suggested connections and suggested schematic below. To use the Net tool, click on the pin of a symbol to start the net and then click on the pin of the component you want to connect to.
16. Save your schematic.

Suggested Board Connections

Arduino Shield Pin	Component Connection
D3	R1
D5	R2
D6	R3
D9	R4
D10	R5
D11	R6
GND	All LED cathodes

Suggested Schematic

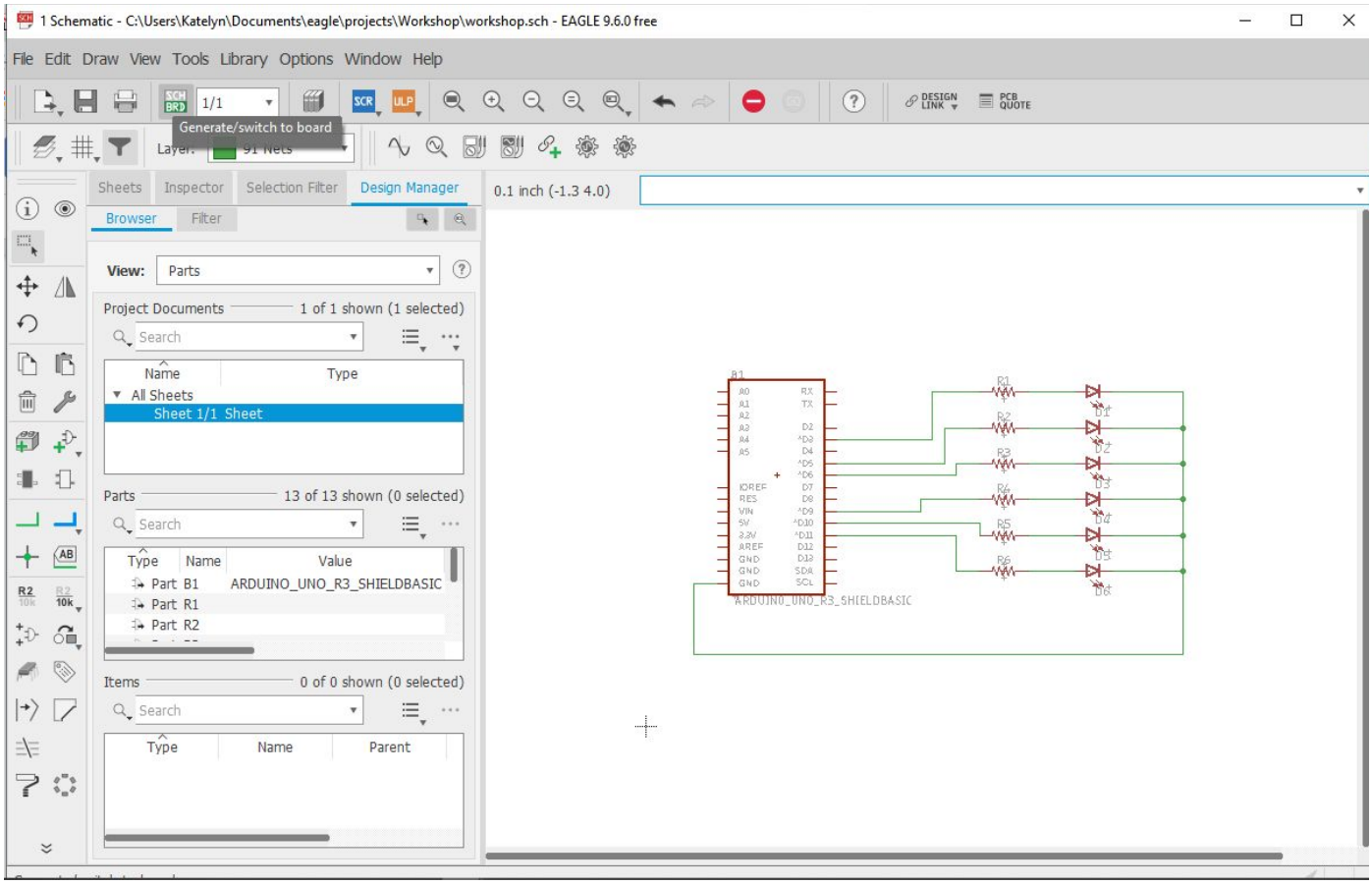


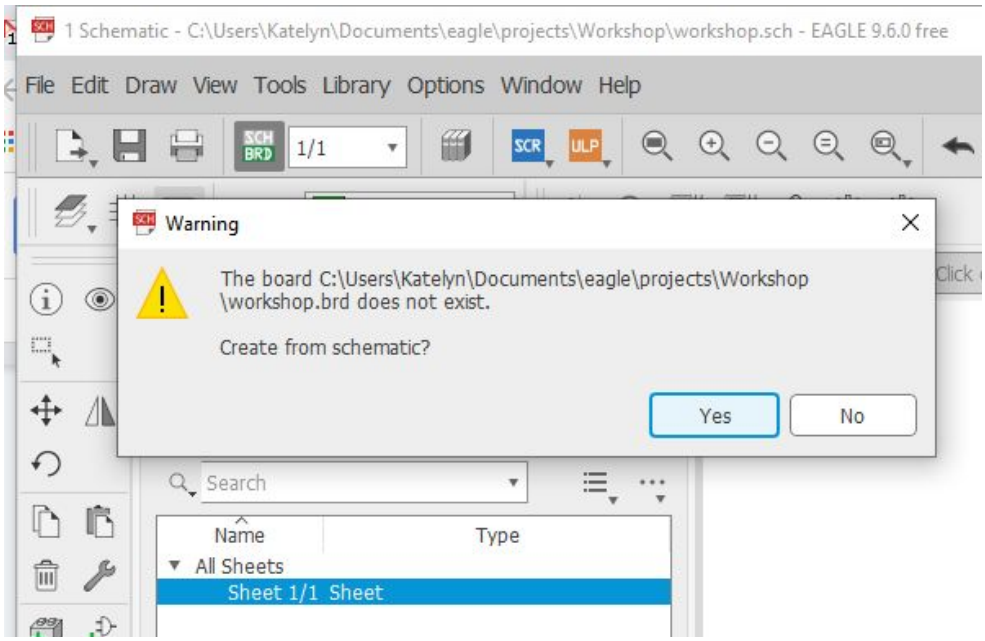
NOTE: There are many possible ways to layout the schematic (i.e., different pin connections and organizations of symbols). This schematic layout will make laying out the board easy and is therefore suggested.

Board Layout

Now that the schematic is complete, we can start the board layout.

17. To create the board, press the “Generate/switch to board” button in the top menu. Select “Yes” in the pop up warning to create the board from the schematic. A new Board window will open.

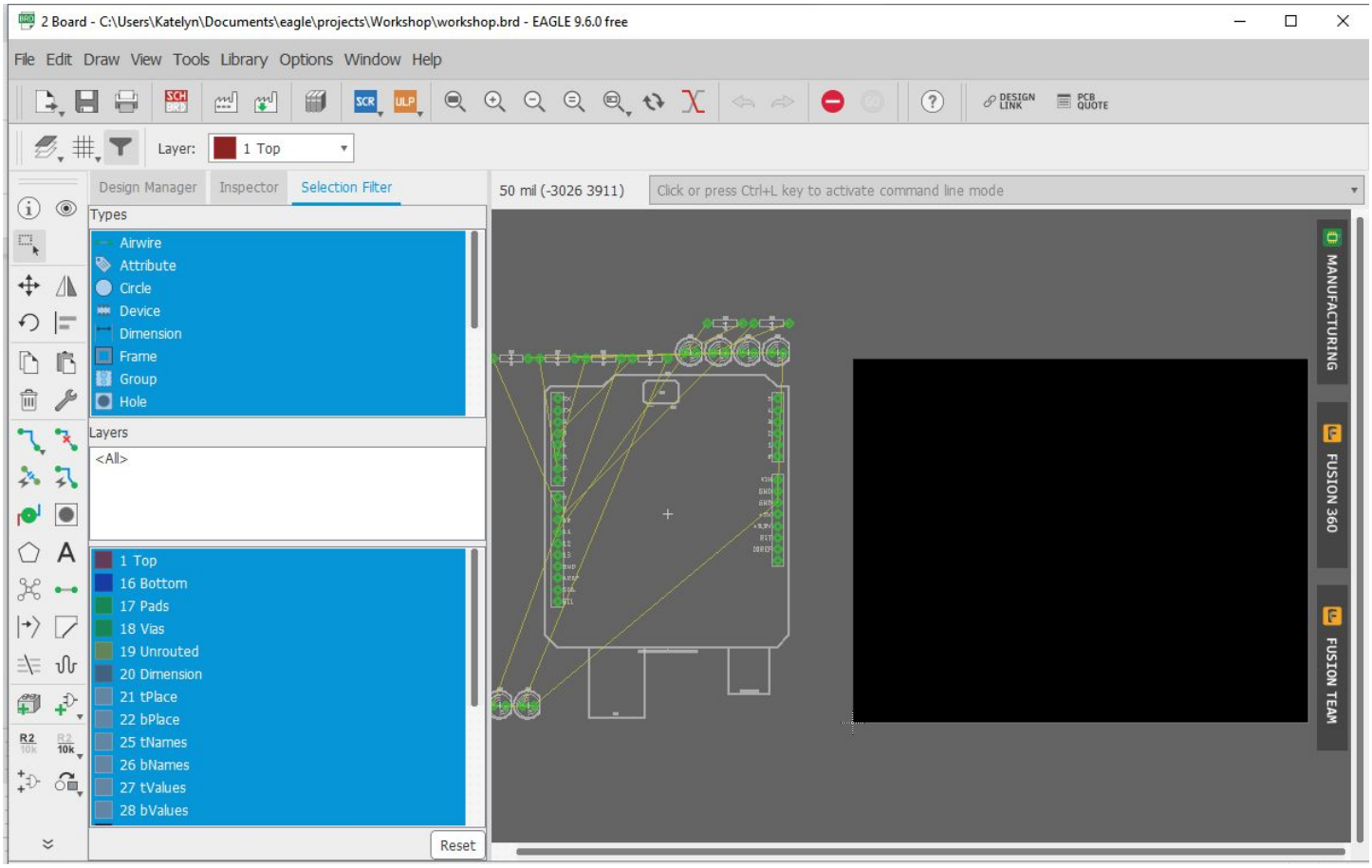




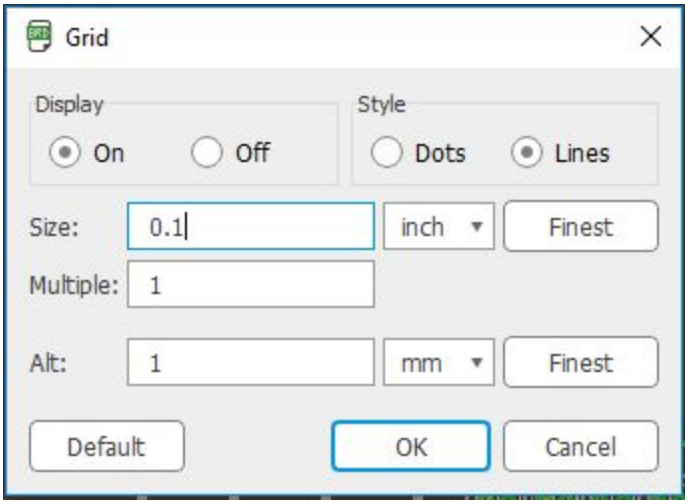
The board window will show the footprints of all the components you had in your schematic. The green circles represent copper pads where through hole components will go in the physical board.

The yellow lines connecting components are called airwires and they represent the connections we made in the schematic. In laying out the board, we will replace the airwires with traces.

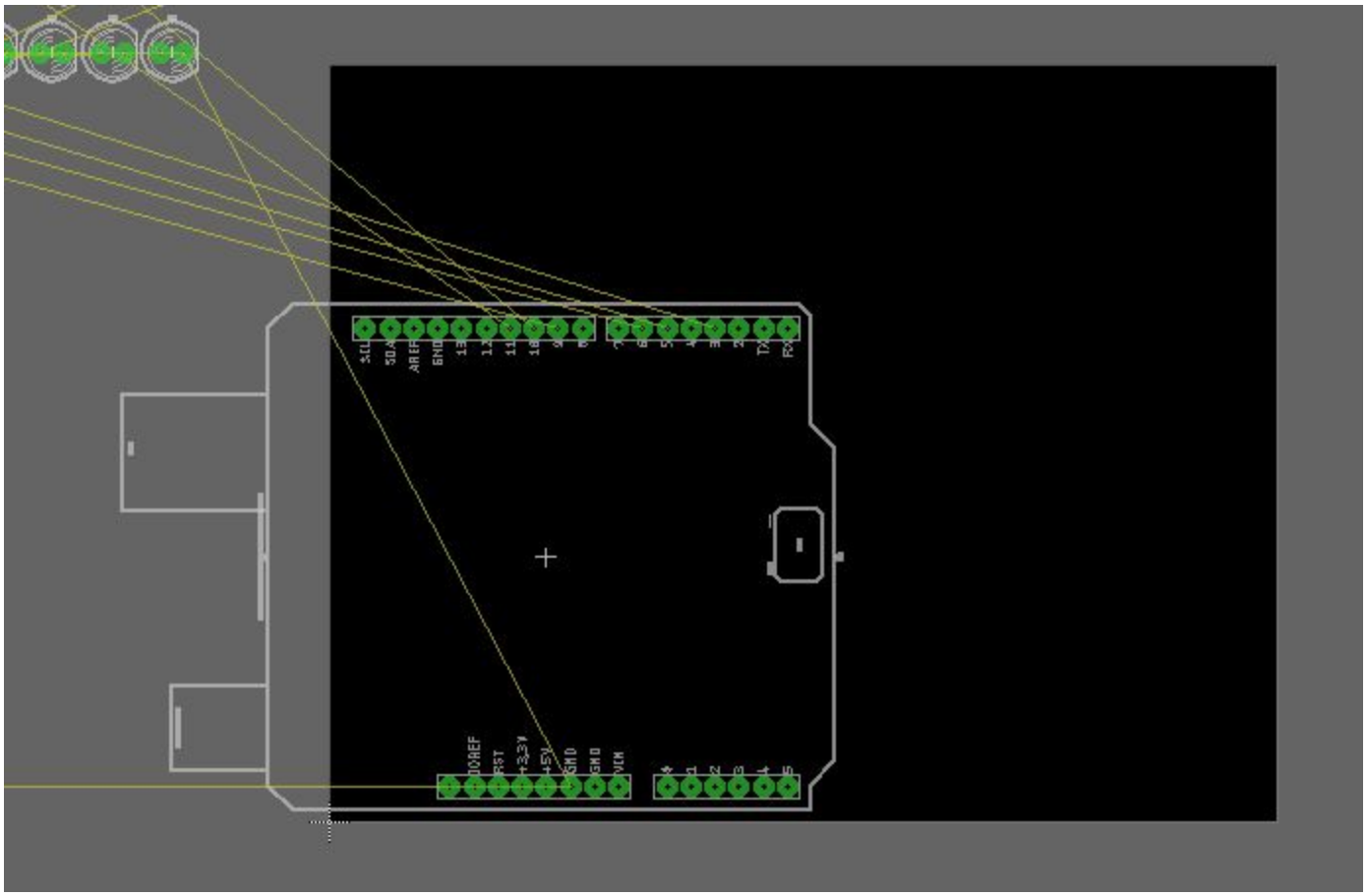
The black area in the board window is the board area. We can adjust the size and shape of the board area based on what we want to fabricate.



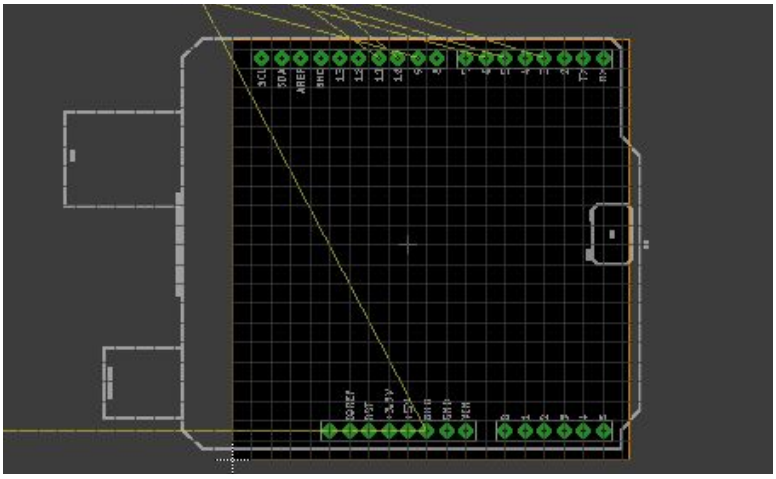
18. Adjust your grid - this is a personal preference.The grid will determine how you can move components. You can choose whether or not to display it.



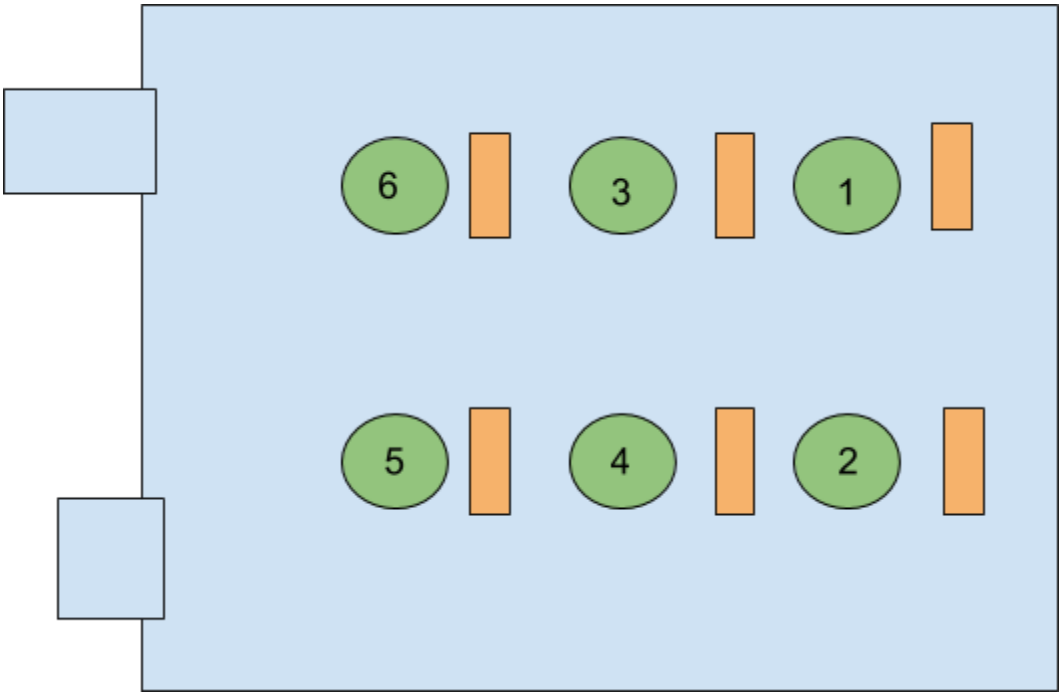
19. Move the Arduino shield into the board area using the move tool. Once you select the shield with the move tool (click on the plus in the middle of the shield outline) you can right click to rotate the shield before placing it. We're going to let the USB and ethernet ports hang off the edge. Since this will be stacking on top of an arduino, we just need to make sure all of our header pins will be in the board profile.

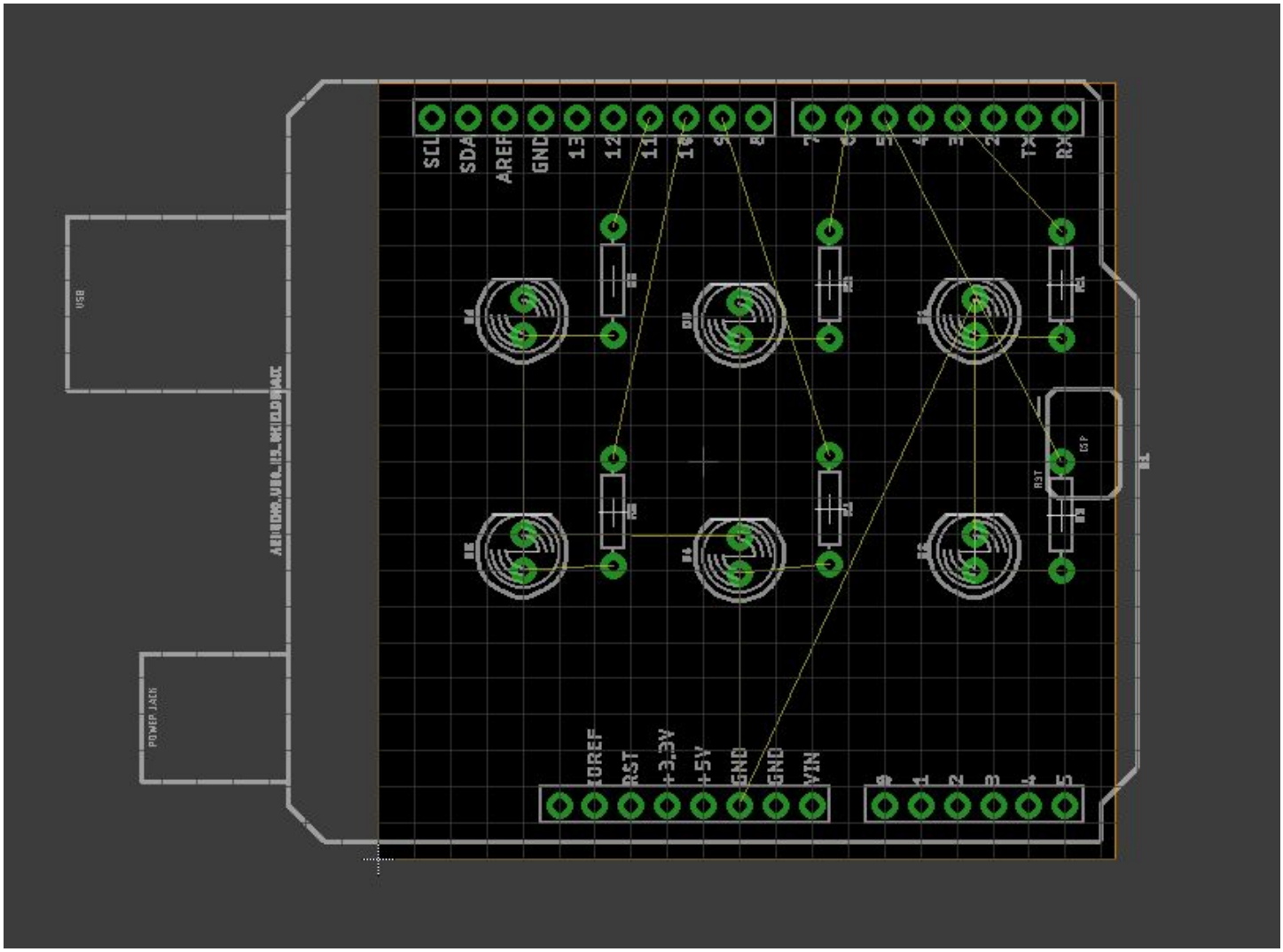


20. Adjust the board size using the move tool so it fits the profile of the arduino. With the move tool selected, click on an edge of the board and drag it in towards the shield. You can also right click on an edge of the board and select properties. In the properties window you can adjust the position of the edge numerically.



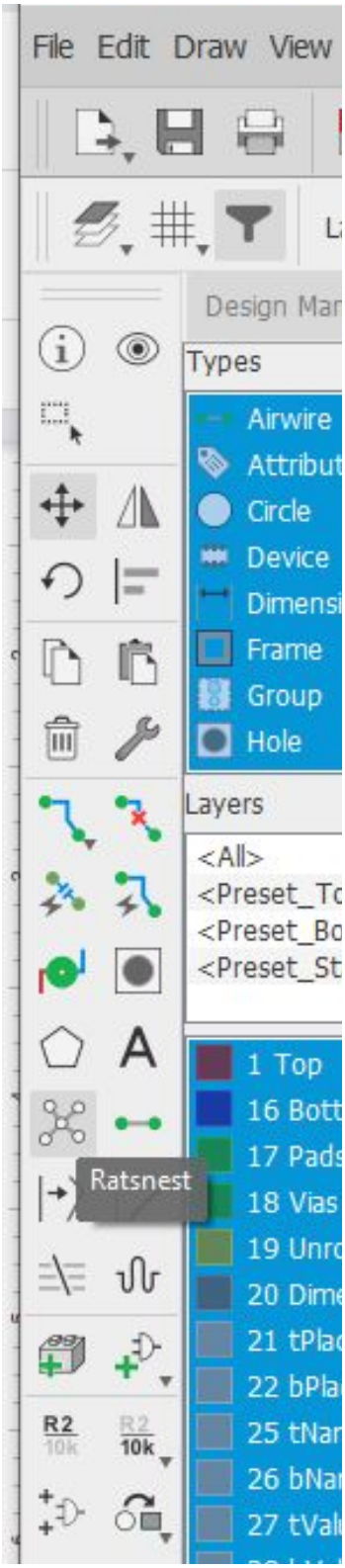
21. Place your remaining components inside your board area using the move tool following the suggested layout. Zoom in to see the component designations (e.g., D3 or R1). It's ultimately up to you how you want to place your components but you want to be able to make connections where all the airwires are without crossing connections and you want your connections to be as direct as possible.
    A. Right click to rotate a component
    B. Use the mouse scroll wheel to zoom in and out
    C. Hold down the scroll wheel to pan around your layout
    D. Hold down the alt key while you move components to move finer increments than your normal grid





The Ratsnest button can be used to clean up airwires. It'll find the most direct connections and adjust for you. The Ratsnest button can be found in the toolbar on the left.

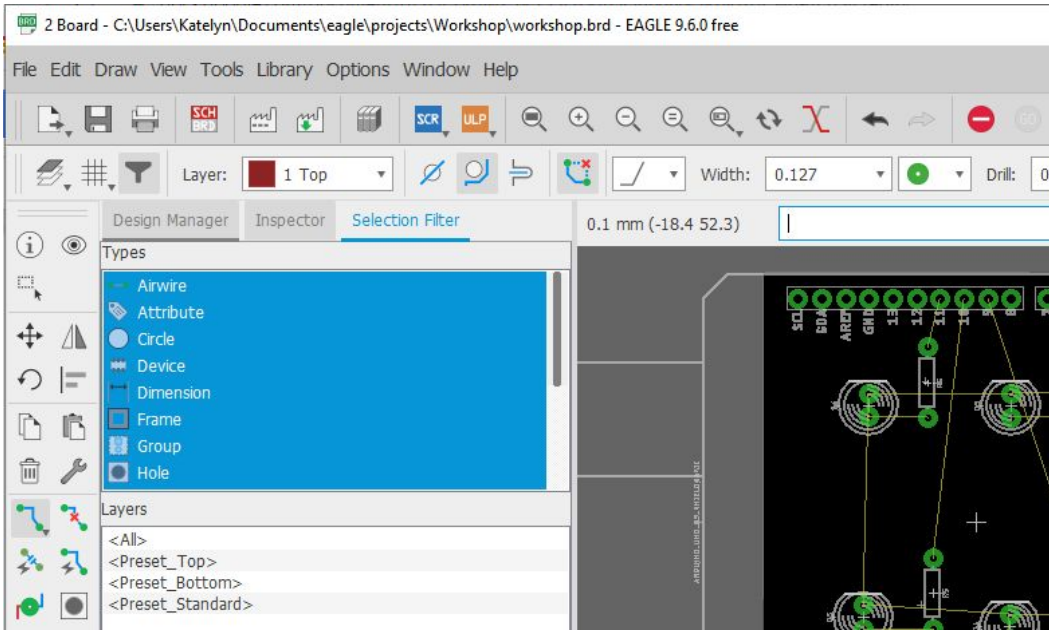
22. Click the Ratsnest button after placing your components in the board area.



Next, we're going to route the board. Routing is the process of placing traces where the airwires are.

The Route Airwire button is located in the left hand toolbar above the Ratsnest button.

23. Select the route button. In the top of the window, adjust the trace settings so that the width is 0.254, the top layer is selected, the walkaround obstacles setting is selected, and the 45 degree bend option is selected.

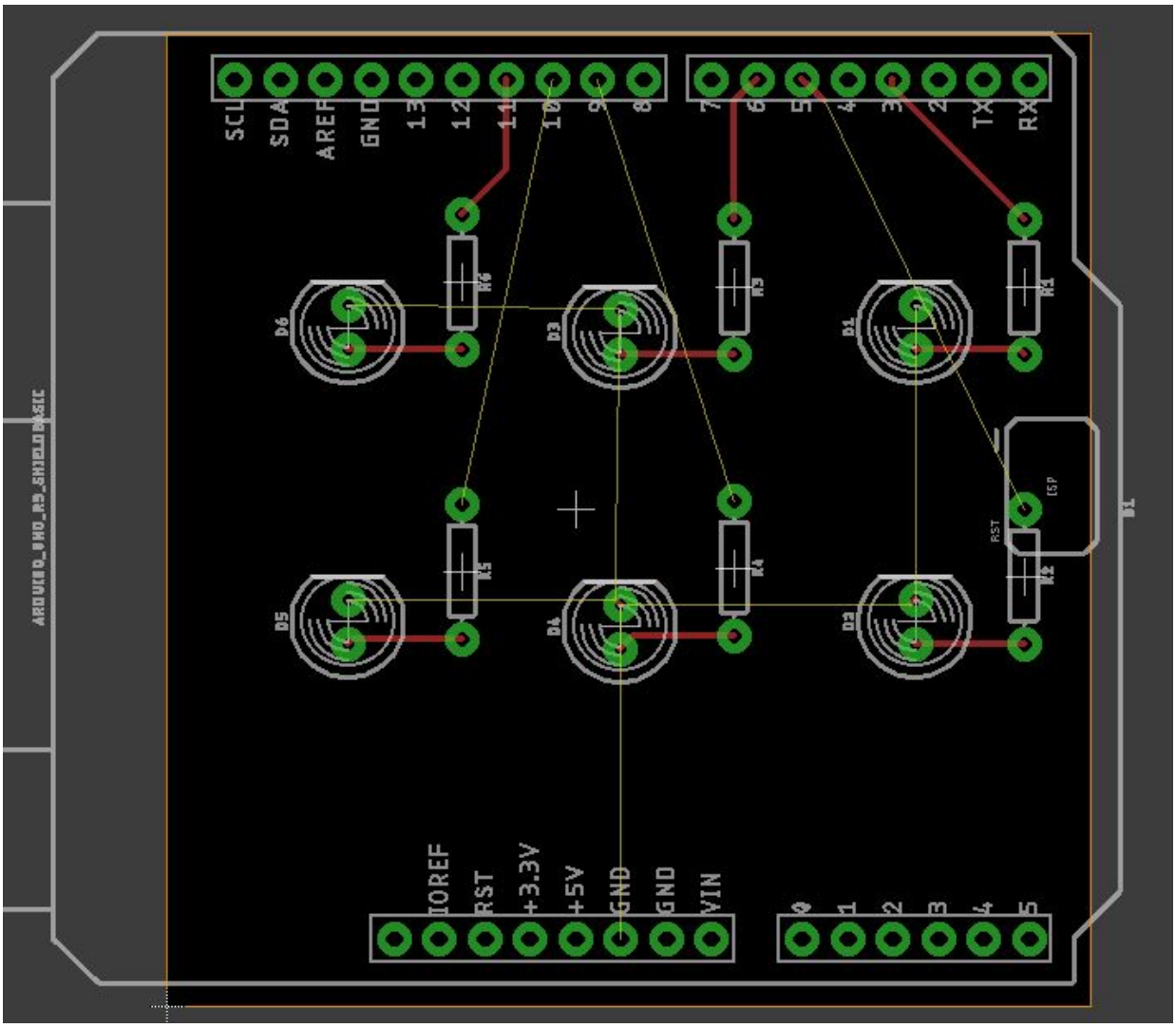


24. Connect R1, R3, and R6 to their arduino pins with the route tool (see example below).
    a. Click inside a pad to start a trace and end on another pad.

25. Connect D6 to R6, D3 to R3, D1 to R1, D5 to R5, D4 to R4, and D2 to R2 with the route tool

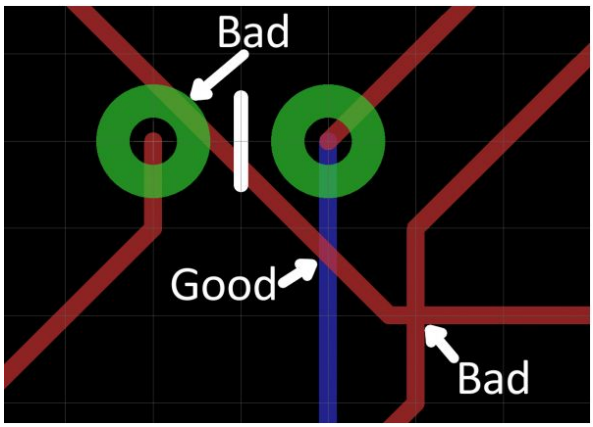
You can change trace directions at 45 degree angles. Be sure to keep some distance between the traces and the pins

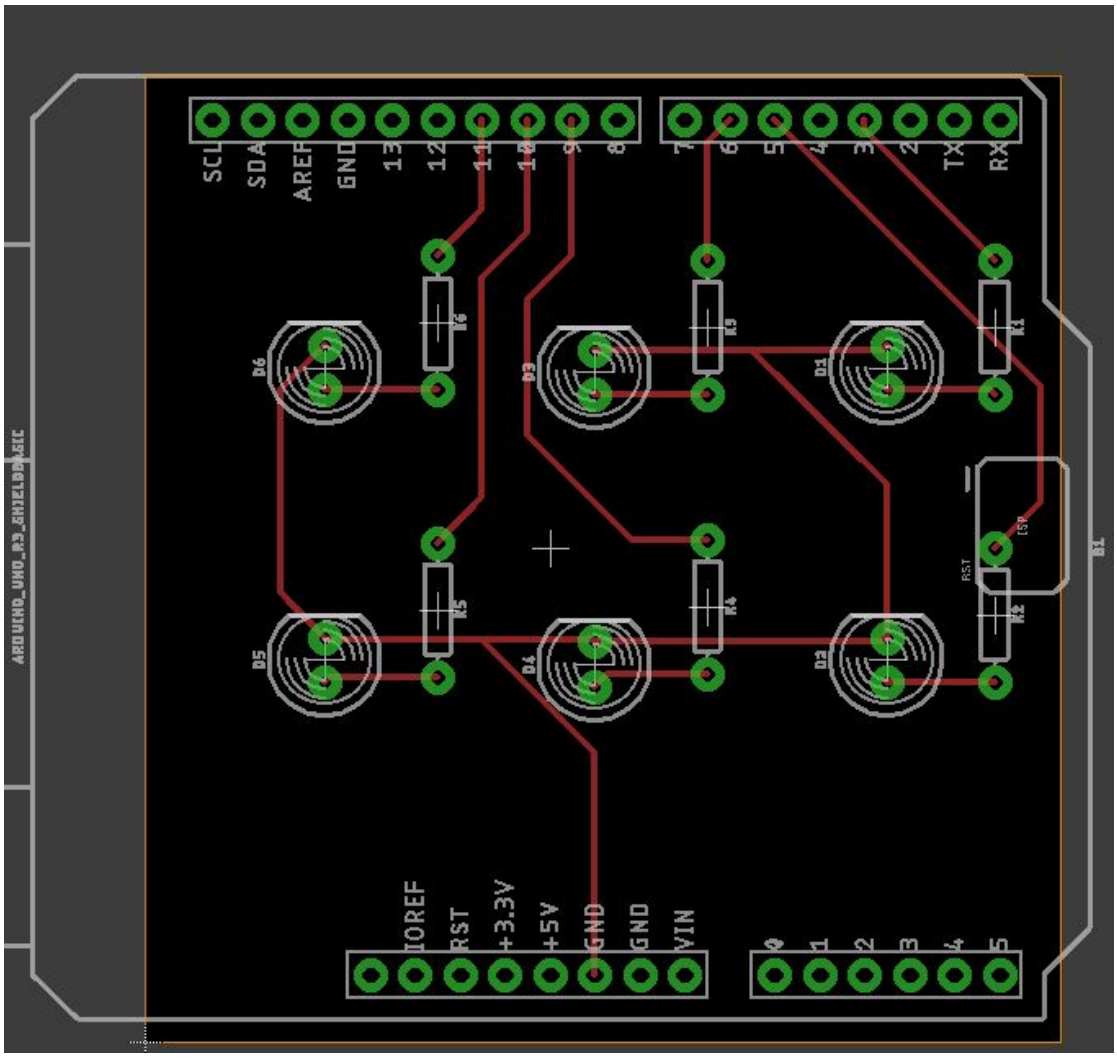
You can use the ripup tool to the right of the route tool to remove any traces you don't like. You can't use the delete tool to get rid of traces.



26. Strategically place the remaining traces. An example full board layout is shown below.
    a. Try to keep routing as direct as possible
    b. Don't cross your trace with another
    c. Avoid routing under components when possible

In the picture below, the different color traces (red and blue) represent traces on different layers of the board and therefore it's okay for them to cross. We're making a 1 layer board so none of our traces should cross.

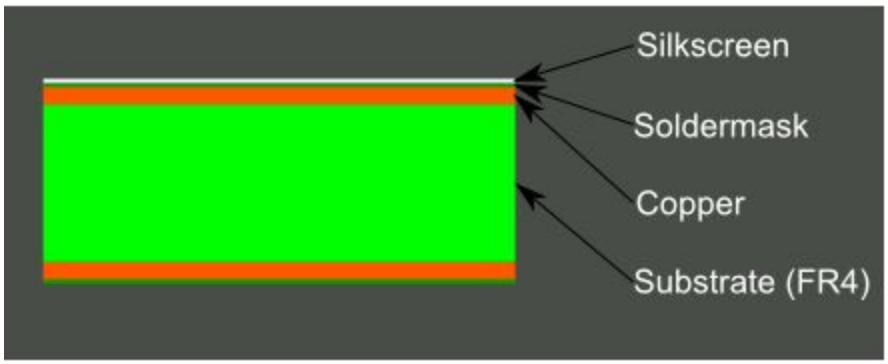




There should be no more visible airwires when you're done routing.

All the traces we just made will be on the top copper layer of the board. On top of that layer is the soldermask. This is what makes most PCBs green. The white writing on top of the soldermask is called the silkscreen.

Board Layers:

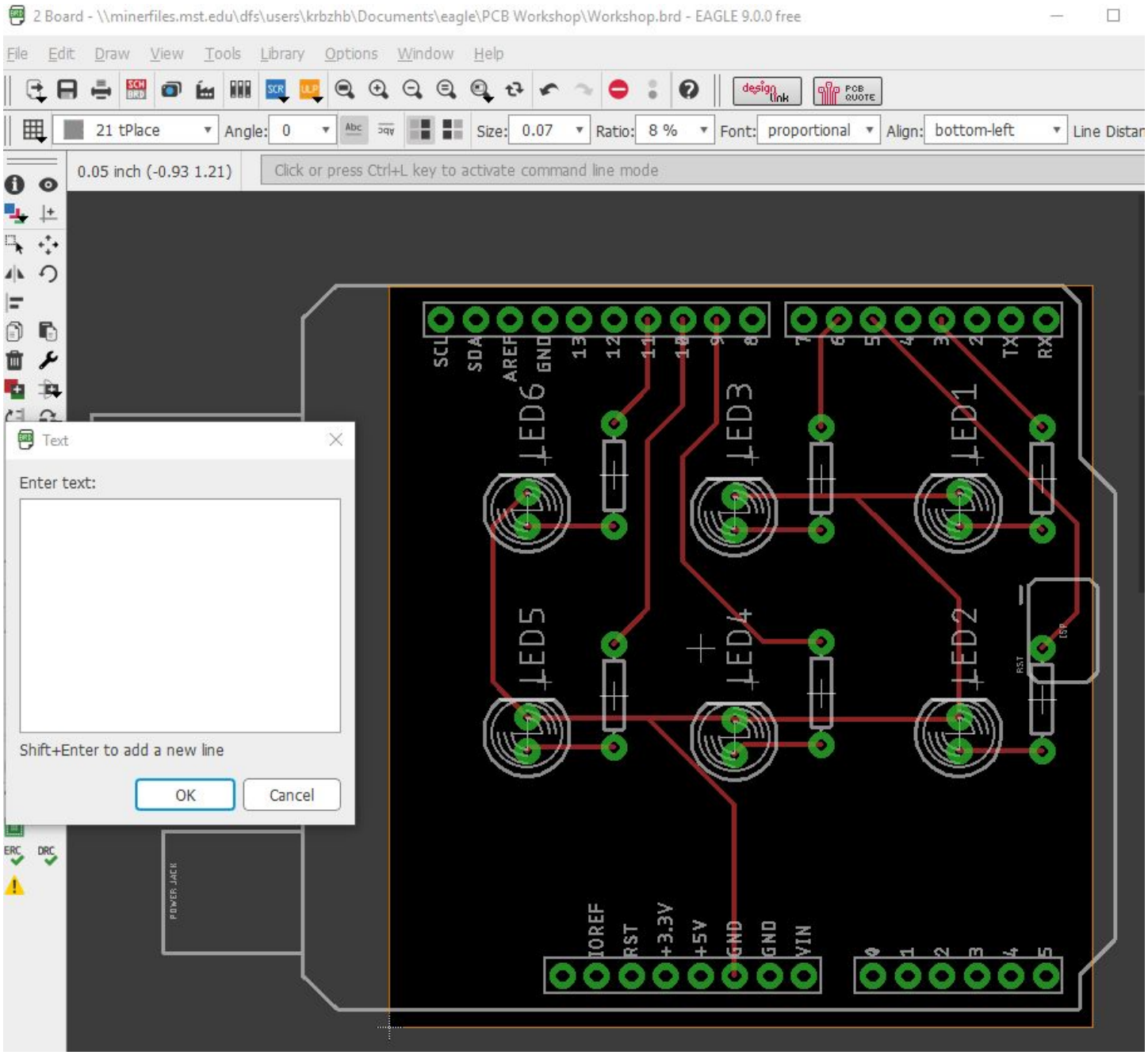


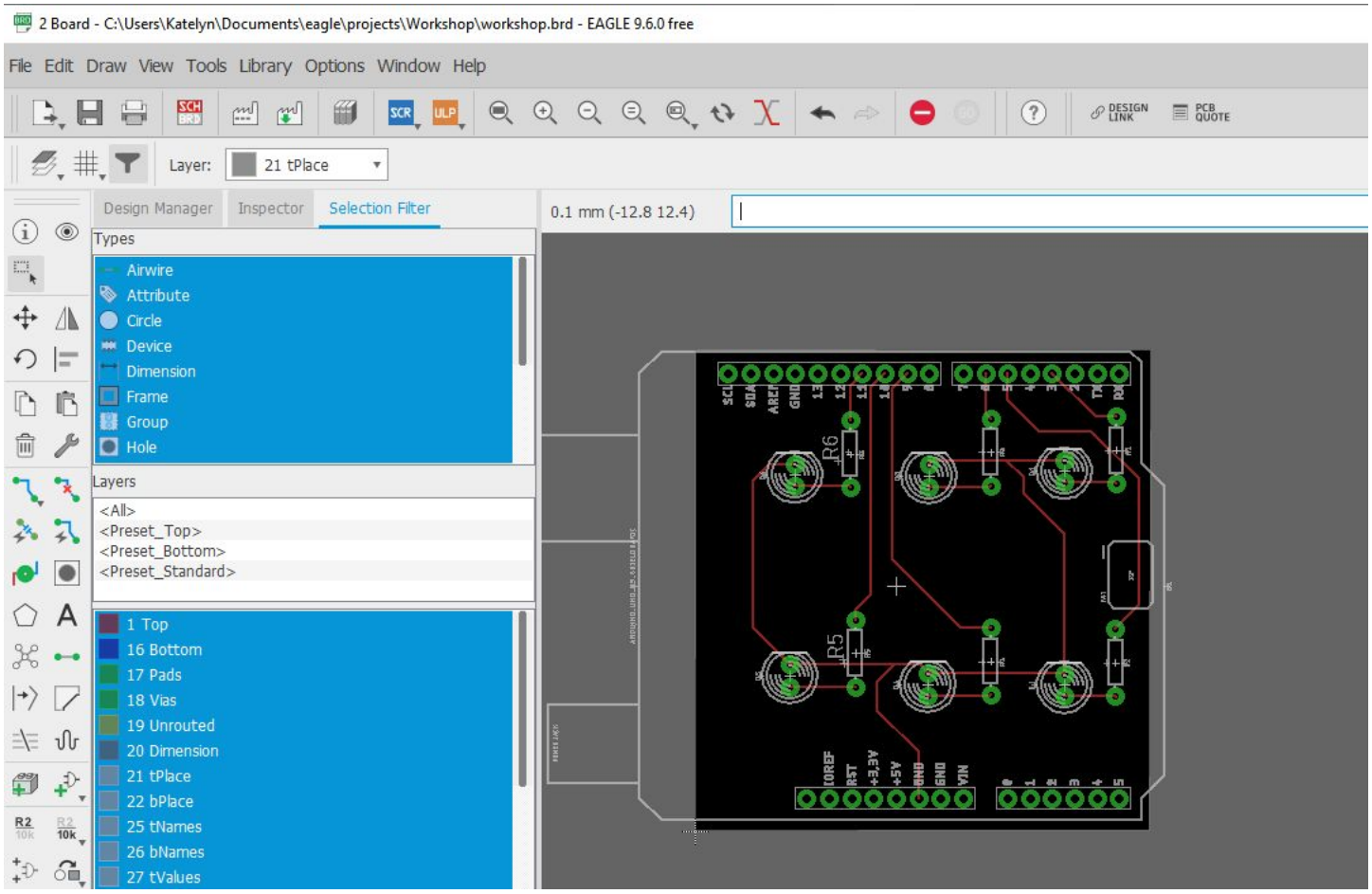
Color	Layer Name	Layer Number	Layer Purpose
	Top	1	Top layer of **copper**
	Bottom	16	Bottom layer of **copper**
	Pads	17	Through-hole pads. Any part of the green circle is exposed **copper** on *both* top and bottom sides of the board.
	Vias	18	Vias. Smaller copper-filled drill holes used to route a signal from top to bottom side. These are usually covered over by soldermask. Also indicates **copper** on both layers.
	Unrouted	19	Airwires. Rubber-band-like lines that show which pads need to be connected.
	Dimension	20	Outline of the board.
	tPlace	21	**Silkscreen** printed on the top side of the board.
	bPlace	22	**Silkscreen** printed on the bottom side of the board.
	tOrigins	23	Top origins, which you click to move and manipulate an individual part.
	bOrigins	24	Origins for parts on the bottom side of the board.
/ / Hatch	tStop	29	Top stopmask. These define where **soldermask** should *not* be applied.
\ \ Hatch	bStop	30	Absent **soldermask** on the bottom side of the board.
	Holes	45	Non-conducting (not a via or pad) holes. These are usually drill holes for stand-offs or for special part requirements.
	tDocu	51	Top documentation layer. Just for reference. This might show the outline of a part, or other useful information.

27. Add text on the silkscreen to label your components. Click on the text button. Type in your label. Click okay and then change the layer to 21 tPlace by finding it in the drop down menu at the top of the window before placing your label next to the correct component on the board

Typically we label our components on the silkscreen so we know what components to put where during assembly.

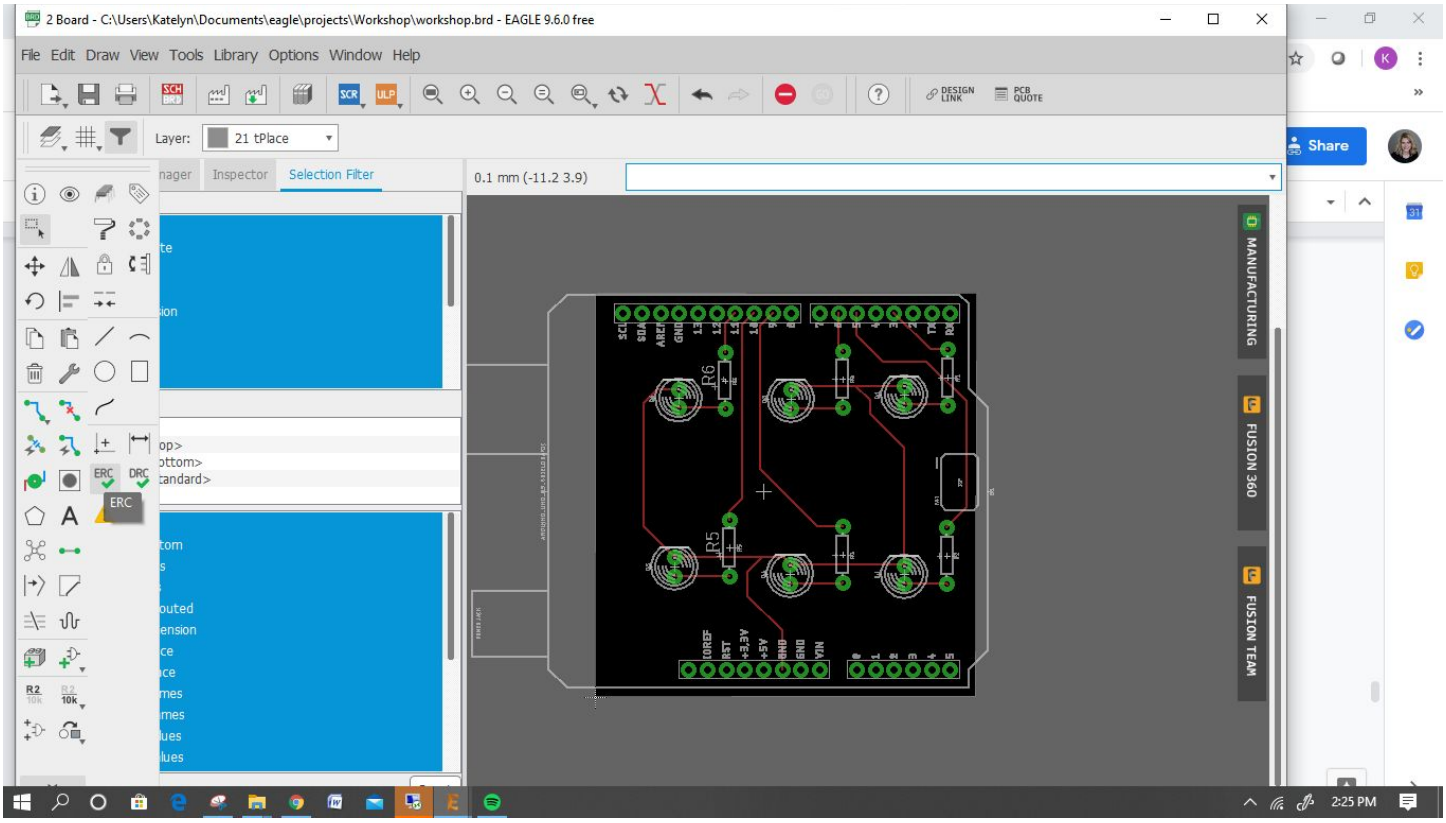
28. Save your board.


2 Board - \\minerfiles.mst.edu\dfs\users\krbzhb\Documents\eagle\PCB Workshop\Workshop.brd - EAGLE 9.0.0 free
File Edit Draw View Tools Library Options Window Help
21 tPlace
Angle: 0
Size: 0.07
Ratio: 8 %
Font: proportional
Align: bottom-left
0.05 inch (-0.93 1.21)
Click or press Ctrl+L key to activate command line mode
Text
Enter text:
Shift+Enter to add a new line
OK
Cancel
LED6
LED3
LED1
LED5
LED4
LED2
SCL
SDA
AREF
GND
13
12
11
10
9
8
7
6
5
4
3
2
TX
RX
IOREF
RST
+3.3V
+5V
GND
GND
VIN
POWER JACK

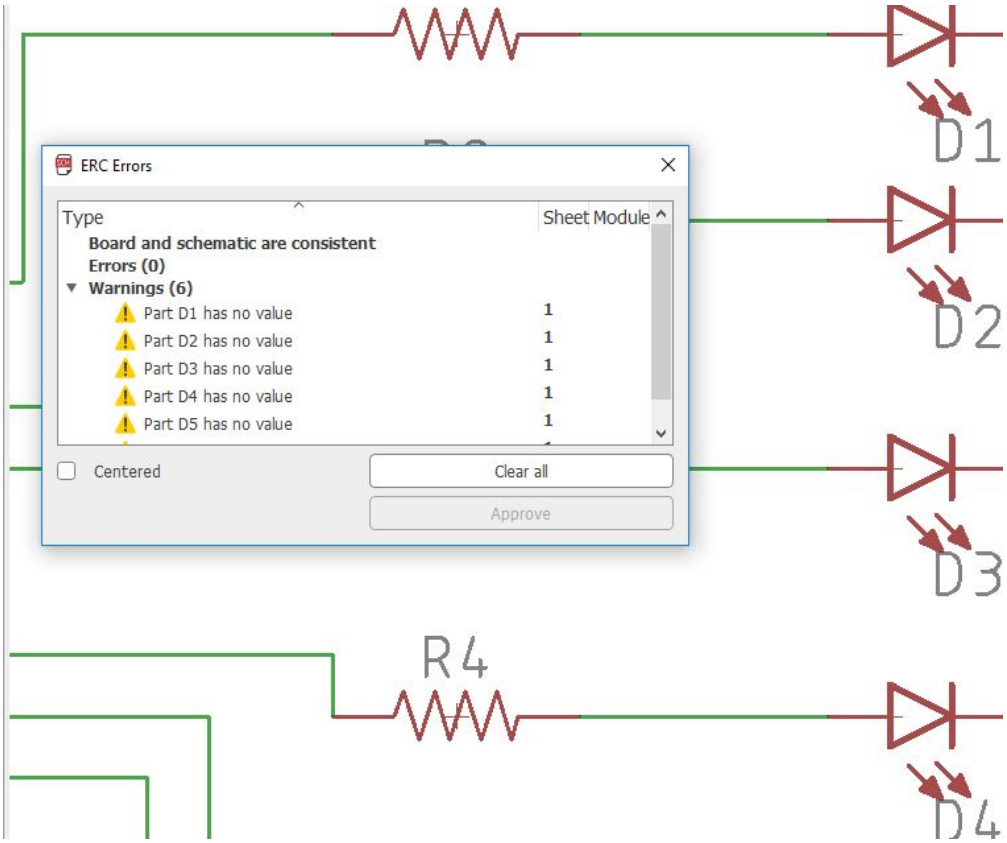

2 Board - C:\Users\Katelyn\Documents\eagle\projects\Workshop\workshop.brd - EAGLE 9.6.0 free
File Edit Draw View Tools Library Options Window Help
Layer: 21 tPlace
Design Manager
Inspector
Selection Filter
Types
Airwire
Attribute
Circle
Device
Dimension
Frame
Group
Hole
Layers
<All>
<Preset_Top>
<Preset_Bottom>
<Preset_Standard>
1 Top
16 Bottom
17 Pads
18 Vias
19 Unrouted
20 Dimension
21 tPlace
22 bPlace
25 tNames
26 bNames
27 tValues
0.1 mm (-12.8 12.4)
R6
R5

Finishing Up

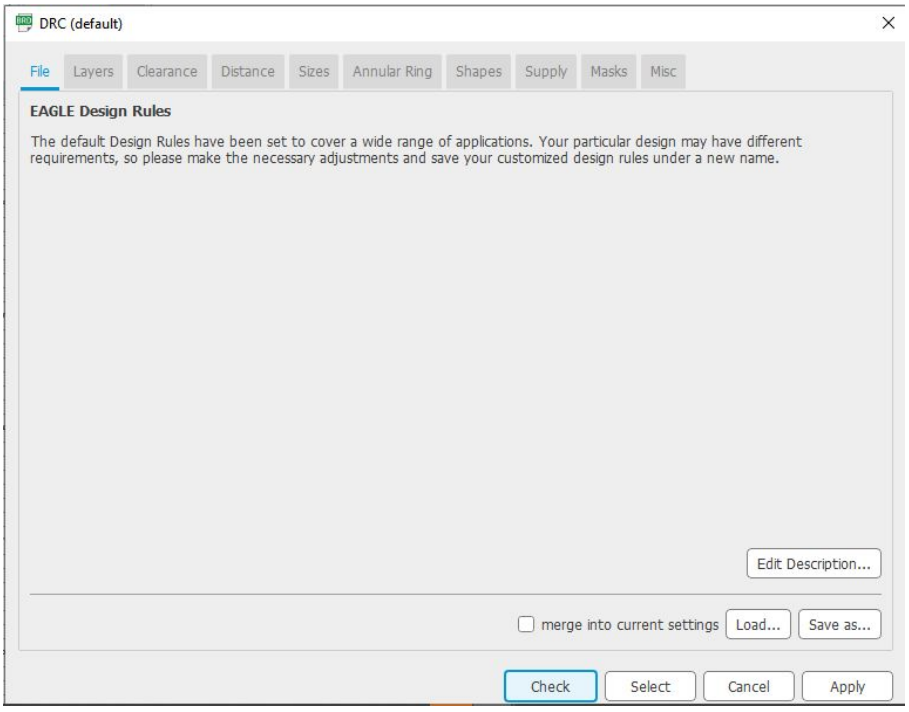
PCB design software has built in checks that you can run to make sure that a PCB manufacturer will be able to make your board. These checks look at things like if your traces are too close to pads or to each other.



29. Check your board design.Hit the ERC button at the bottom left of your toolbar. You might need to hit the down arrow at the bottom of the toolbar to show the other tools. You may see warnings about the LEDs not having values. You can clear these warnings.

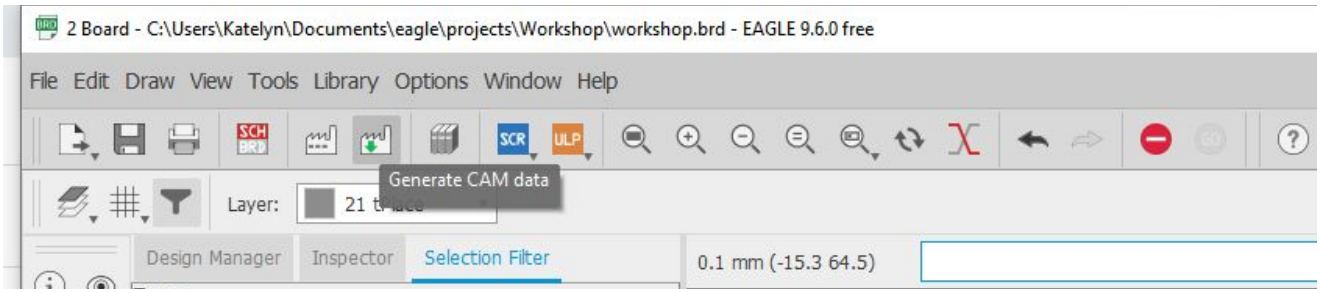


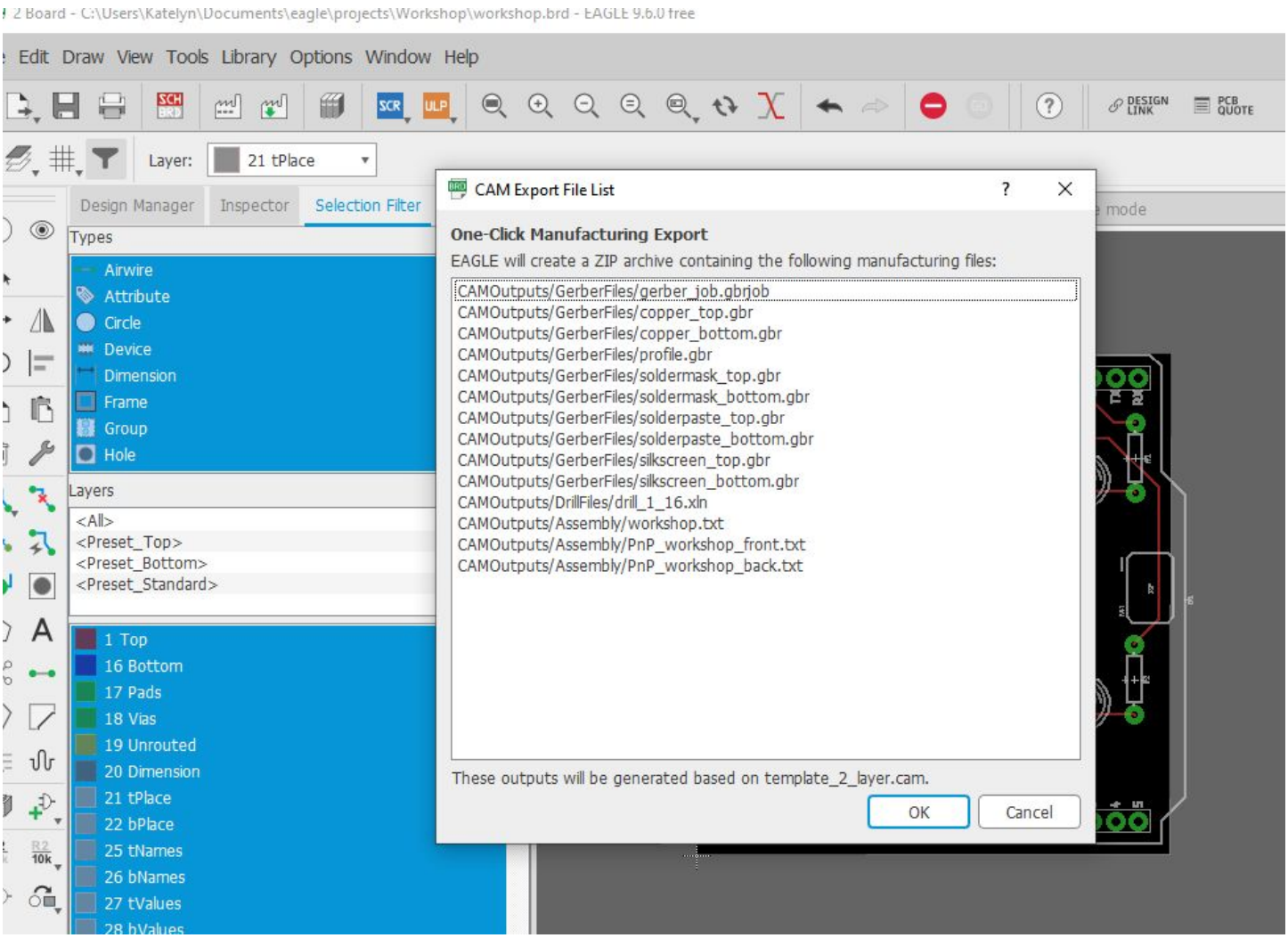
30. In the board layout view, in the DRC button next to the ERC button. This will check your layout for errors. Hit “Check” in the pop up window. This will run the default design rule check. PCB manufacturers also have their own DRCs that you can download and then run in your PCB design software.



1. Generate the gerber files. Click on the generate CAM data button. Then click okay.

Gerber files are what we send to PCB manufacturers to make boards. They provide the mechanical description of each board layer.





Additional Resources

Making your own Custom components:

There will be times when you can't find a pre-made library for a component that you need. In this case you need to use the datasheet to make it yourself. The following tutorial walks through the steps.

- https://www.autodesk.com/products/eagle/blog/library-basics-part-1-creating-first-package-autodesk-eagle/
- https://learn.adafruit.com/ktowns-ultimate-creating-parts-in-eagle-tutorial/adding-%3Ename-and-%3Evalue-to-your-symbol

Routing on 2 or more layers:

Sometimes, you can't route all of your traces without crossing other traces, which isn't allowed, or making really round about paths. In these cases, you can route on multiple layers (i.e., you can put traces on a top layer and a bottom layer).

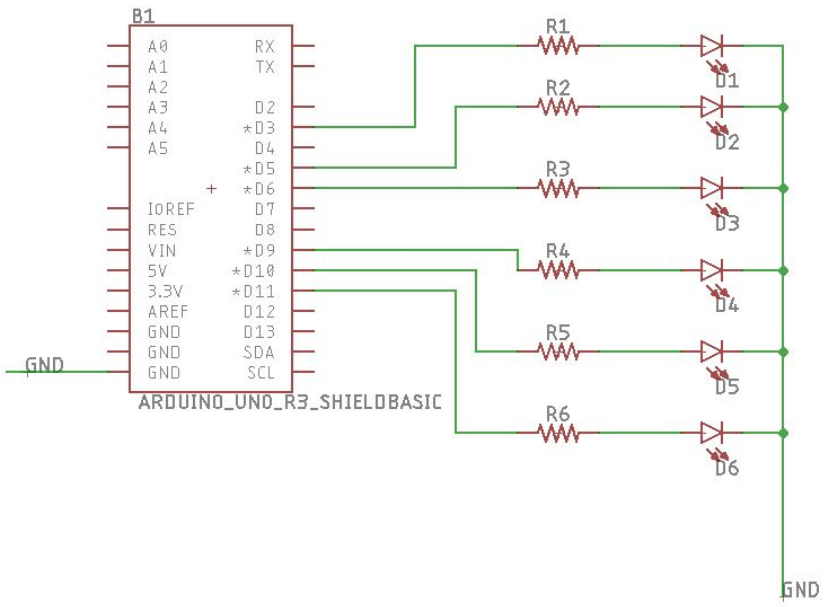
You can use vias to change layers.

Check out the following tutorials for more information.

- https://learn.sparkfun.com/tutorials/using-eagle-board-layout
- http://dangerousprototypes.com/blog/2012/07/18/eagle-polygons/

Enhancing your schematic:

Use the name tool to name nets and connect them without running a net wire between them. When you name two nets the same, Eagle will ask you if you want to connect them. This will clean up your schematic and make it easier during layout to understand what you're connecting.



You can also add values to your components in your schematic.

- https://www.autodesk.com/products/eagle/blog/schematic-basics-part-2-nets-and-values/
- https://learn.sparkfun.com/tutorials/using-eagle-schematic/tips-and-tricks

PCB Fabrication

In order to fabricate a PCB, you usually sent it to a fab house. Different fab houses have different requirements you must meet for them to fabricate your board. You can find these requirements on their website. Fab houses are have different costs and production times.

Here are some fab house options:

- https://easyeda.com/
- https://www.sunstone.com/
- https://www.4pcb.com/
- https://oshpark.com/

Additional Design Tutorials and Example Projects:

- https://learn.sparkfun.com/tutorials/designing-pcbs-advanced-smd
- https://learn.sparkfun.com/tutorials/arduino-shields
- https://circuitdigest.com/diy-pcb-projects